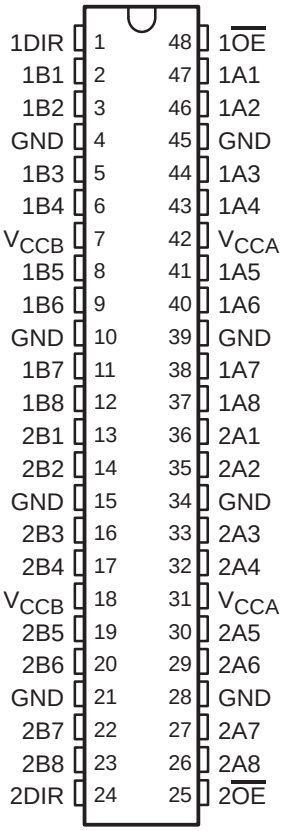
- **Control Inputs V_{IH}/V_{IL} Levels are Referenced to V_{CCA} Voltage**
- **V_{CC} Isolation Feature − If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State**
- **Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications**
- **Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range**
- **I_{off} Supports Partial-Power-Down Mode Operation**

DGG OR DGV PACKAGE
(TOP VIEW)



description/ordering information

This 16-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

The SN74LVC16T245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the outputs so the buses are effectively isolated.

The SN74LVC16T245 is designed so that the control pins (1DIR, 2DIR, 1$\overline{OE}$, and 2$\overline{OE}$) are supplied by V_{CCA}.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	TSSOP − DGG	Tape and reel	SN74LVC16T245DGGR	
	TVSOP − DGV	Tape and reel	SN74LVC16T245DGVR	
	VFBGA − GQL	Tape and reel	SN74LVC16T245GQLR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

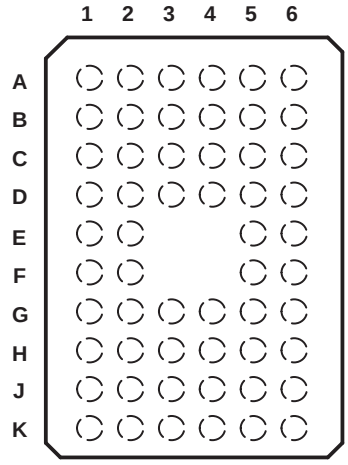
description/ordering information (continued)

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both ports are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

GQL PACKAGE
(TOP VIEW)



terminal assignments

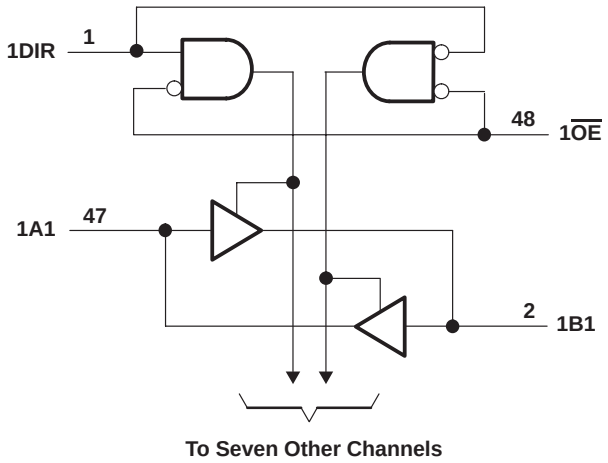
	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	1$\overline{OE}$
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	V_{CCB}	V_{CCA}	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V_{CCB}	V_{CCA}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	2$\overline{OE}$

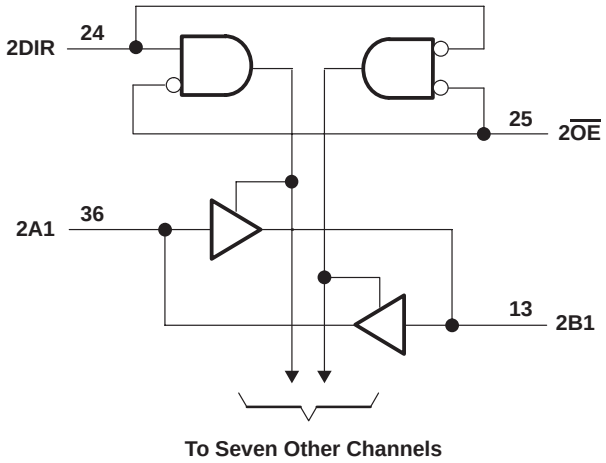
NC − No internal connection

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CCA} and V_{CCB}	−0.5 V to 6.5 V
Input voltage range, V_I (see Note 1): I/O ports (A port)	−0.5 V to 6.5 V
I/O ports (B port)	−0.5 V to 6.5 V
Control inputs	−0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): (A port)	−0.5 V to 6.5 V
(B port)	−0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2): (A port)	−0.5 V to V_{CCA} + 0.5 V
(B port)	−0.5 V to V_{CCB} + 0.5 V
Input clamp current, I_{IK} (V_I < 0)	−50 mA
Output clamp current, I_{OK} (V_O < 0)	−50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CCA}, V_{CCB}, and GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	70°C/W
DGV package	58°C/W
GQL package	42°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

PRODUCT PREVIEW

recommended operating conditions (see Notes 4 through 6)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.65	5.5	V
V_{CCB}					1.65	5.5	
V_{IH}	High-level input voltage	Data inputs (see Note 7)	1.65 V to 1.95 V		$V_{CCI} \times 0.65$		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		$V_{CCI} \times 0.7$		
V_{IL}	Low-level input voltage	Data inputs (see Note 7)	1.65 V to 1.95 V			$V_{CCI} \times 0.35$	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			$V_{CCI} \times 0.3$	
V_{IH}	High-level input voltage	DIR (Referenced to V_{CCA}) (see Note 8)	1.65 V to 1.95 V		$V_{CCA} \times 0.65$		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		$V_{CCA} \times 0.7$		
V_{IL}	Low-level input voltage	DIR (Referenced to V_{CCA}) (see Note 8)	1.65 V to 1.95 V			$V_{CCA} \times 0.35$	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			$V_{CCA} \times 0.3$	
V_I	Input voltage				0	5.5	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-State			0	3.6	
I_{OH}	High-level output current			1.65 V to 1.95 V		−4	mA
				2.3 V to 2.7 V		−8	
				3 V to 3.6 V		−24	
				4.5 V to 5.5 V		−32	
I_{OL}	Low-level output current			1.65 V to 1.95 V		4	mA
				2.3 V to 2.7 V		8	
				3 V to 3.6 V		24	
				4.5 V to 5.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	Data inputs	1.65 V to 1.95 V			20	ns/V
			2.3 V to 2.7 V			20	
			3 V to 3.6 V			10	
			4.5 V to 5.5 V			5	
T_A	Operating free-air temperature				−40	85	°C

NOTES: 4. V_{CCI} is the V_{CC} associated with the data input port.
5. V_{CCO} is the V_{CC} associated with the output port.
6. All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
7. For V_{CCI} values not specified in the data sheet, $V_{IH(min)} = V_{CCI} \times 0.7$ V, $V_{IL(max)} = V_{CCI} \times 0.3$ V.
8. For V_{CCI} values not specified in the data sheet, $V_{IH(min)} = V_{CCA} \times 0.7$ V, $V_{IL(max)} = V_{CCA} \times 0.3$ V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Notes 9 and 10)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C			−40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
V_{OH}		I_{OH} = −100 μA,	$V_I = V_{IH}$	1.65 V to 4.5 V	1.65 V to 4.5 V				V_{CCO} − 0.1 V		V
		I_{OH} = −4 mA,	$V_I = V_{IH}$	1.65V	1.65 V				1.2		
		I_{OH} = −8 mA,	$V_I = V_{IH}$	2.3 V	2.3 V				1.9		
		I_{OH} = −24 mA,	$V_I = V_{IH}$	3 V	3 V				2.4		
		I_{OH} = −32 mA,	$V_I = V_{IH}$	4.5 V	4.5 V				3.8		
V_{OL}		I_{OL} = 100 μA,	$V_I = V_{IL}$	1.65 V to 4.5 V	1.65 V to 4.5 V					0.1	V
		I_{OL} = 4 mA,	$V_I = V_{IL}$	1.65 V	1.65 V					0.45	
		I_{OL} = 8 mA,	$V_I = V_{IL}$	2.3 V	2.3 V					0.3	
		I_{OL} = 24 mA,	$V_I = V_{IL}$	3 V	3 V					0.55	
		I_{OL} = 32 mA,	$V_I = V_{IL}$	4.5 V	4.5 V					0.55	
I_I	DIR input	$V_I = V_{CCA}$ or GND		1.65 V to 5.5 V	1.65 V to 5.5 V			±1		±2	μA
I_{off}	A or B port	V_I or V_O = 0 to 5.5 V		0 V	0 to 5.5 V			±1		±2	μA
				0 to 5.5 V	0 V			±1		±2	
I_{OZ}	A or B ports	$V_O = V_{CCO}$ or GND	$\overline{OE} = V_{IH}$	1.65 V to 5.5 V	1.65 V to 5.5 V			±1		±2	μA
I_{CCA}		$V_I = V_{CCI}$ or GND	I_O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V					20	μA
				5 V	0 V					20	
				0 V	5 V					−2	
I_{CCB}		$V_I = V_{CCI}$ or GND	I_O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V					20	μA
				5 V	0 V					−2	
				0 V	5 V					20	
I_{CCA} + I_{CCB}		$V_I = V_{CCI}$ or GND	I_O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V					30	μA
ΔI_{CCA}	A port	One A port at V_{CCA} − 0.6 V, DIR at V_{CCA}, B port = OPEN		3 V to 5.5 V	3 V to 5.5 V					50	μA
	DIR	DIR at V_{CCA} − 0.6 V, B port = OPEN, A port at V_{CCA} or GND								50	
ΔI_{CCB}	B port	One B port at V_{CCB} − 0.6 V, DIR at GND, A port = OPEN		3 V to 5.5 V	3 V to 5.5 V					50	μA
C_i	DIR input	$V_I = V_{CCA}$ or GND		3.3 V	3.3 V						pF
C_{io}	A or B ports	$V_O = V_{CCA/B}$ or GND		3.3 V	3.3 V						pF

NOTES: 9. V_{CCO} is the V_{CC} associated with the output port.
10. V_{CCI} is the V_{CC} associated with the input port.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B									ns
t_{PHL}											
t_{PLH}	B	A									ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A									ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B									ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A									ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B									ns
t_{PZL}											

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B									ns
t_{PHL}											
t_{PLH}	B	A									ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A									ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B									ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A									ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B									ns
t_{PZL}											

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B									ns
t_{PHL}											
t_{PLH}	B	A									ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A									ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B									ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A									ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B									ns
t_{PZL}											

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B									ns
t_{PHL}											
t_{PLH}	B	A									ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A									ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B									ns
t_{PLZ}											
t_{PZH}†	$\overline{OE}$	A									ns
t_{PZL}†											
t_{PZH}†	$\overline{OE}$	B									ns
t_{PZL}†											

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3.3 V	V_{CCA} = V_{CCB} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pdA}†	A port input, B port output	C_L = 0, f = 10 MHz, t_r = t_f =1 ns					pF
	B port input, A port output						
C_{pdB}†	A port input, B port output						
	B port input, A port output						

† Power-dissipation capacitance per transceiver

PRODUCT PREVIEW

power-up considerations

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

1. Connect ground before any supply voltage is applied.
2. Power up V_{CCA}.
3. V_{CCB} can be ramped up along with or after V_{CCA}.

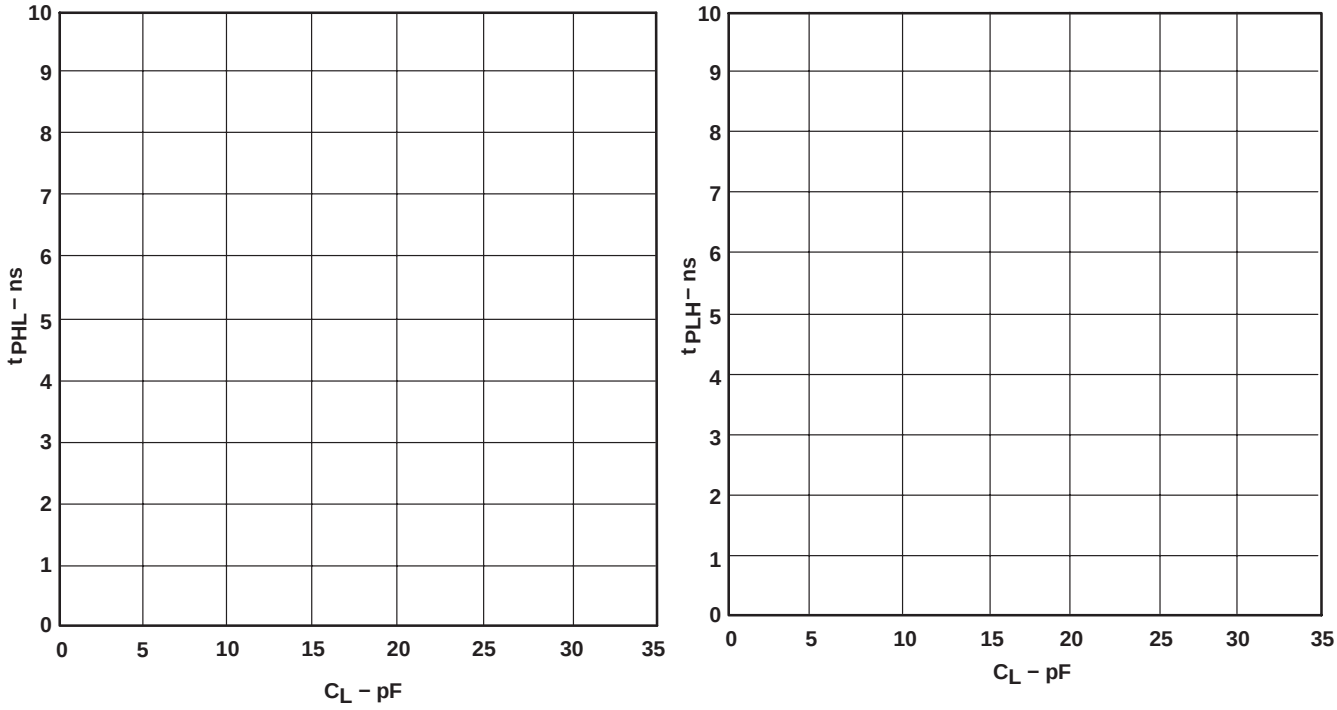
typical total static power consumption (I_{CCA} + I_{CCB})

Table 1

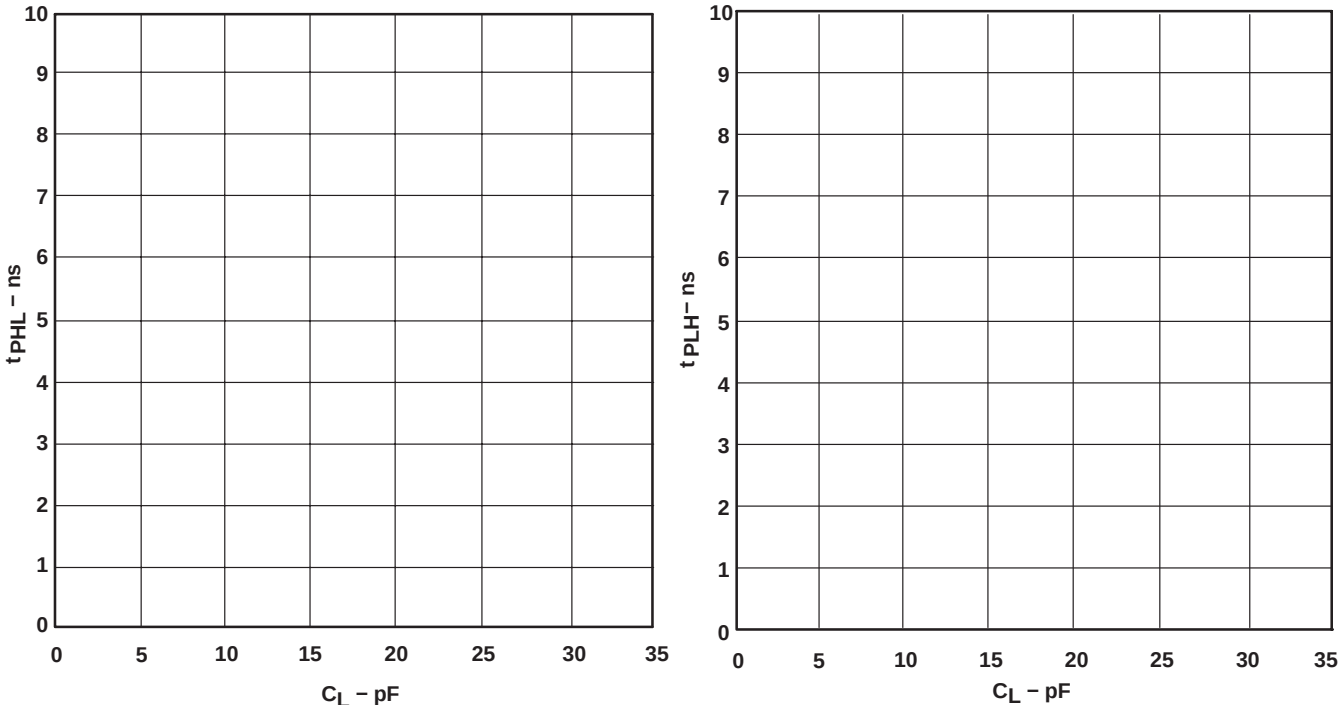
V_{CCB}	V_{CCA}					UNIT
	0 V	1.8 V	2.5 V	3.3 V	5 V	
0 V						μA
1.8 V						
2.5 V						
3.3 V						
5 V						

TYPICAL CHARACTERISTICS

TYPICAL PROPAGATION DELAY (A TO B) vs LOAD CAPACITANCE
$T_A = 25°C$, $V_{CCA} = 1.8$ V



TYPICAL PROPAGATION DELAY (B TO A) vs LOAD CAPACITANCE
$T_A = 25°C$, $V_{CCA} = 1.8$ V

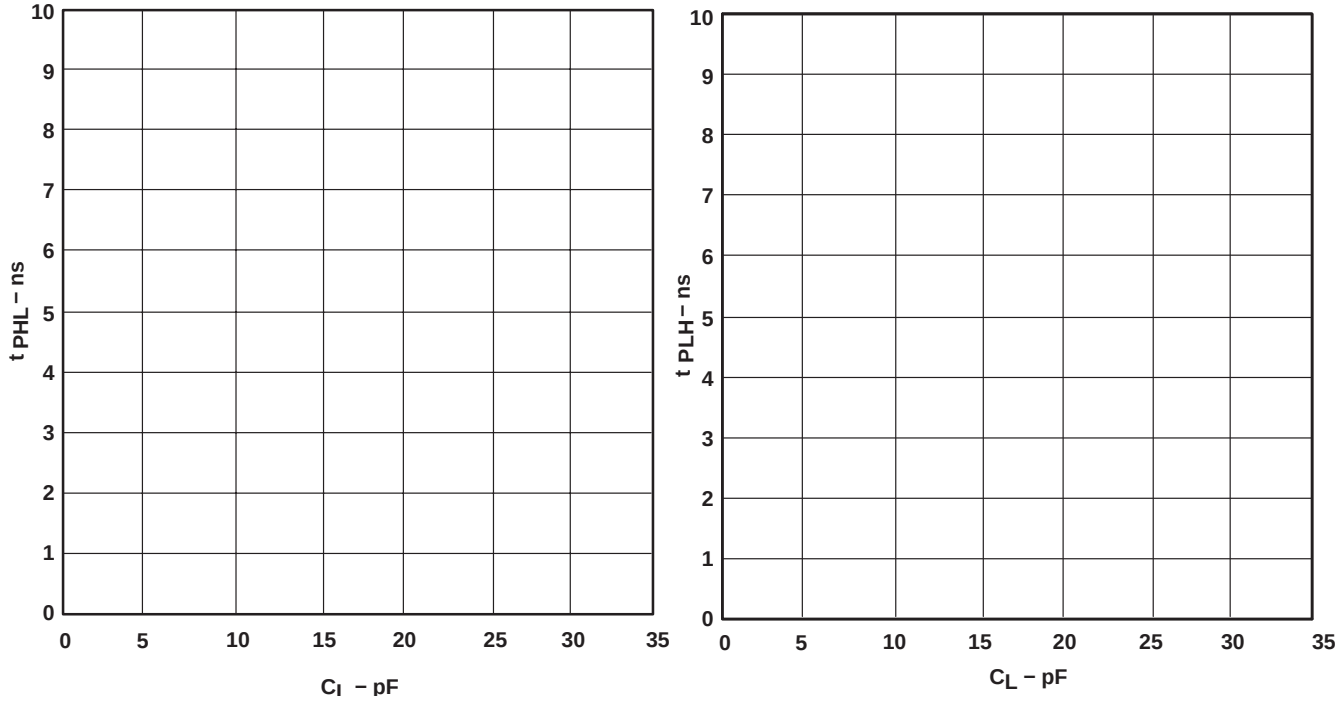


PRODUCT PREVIEW

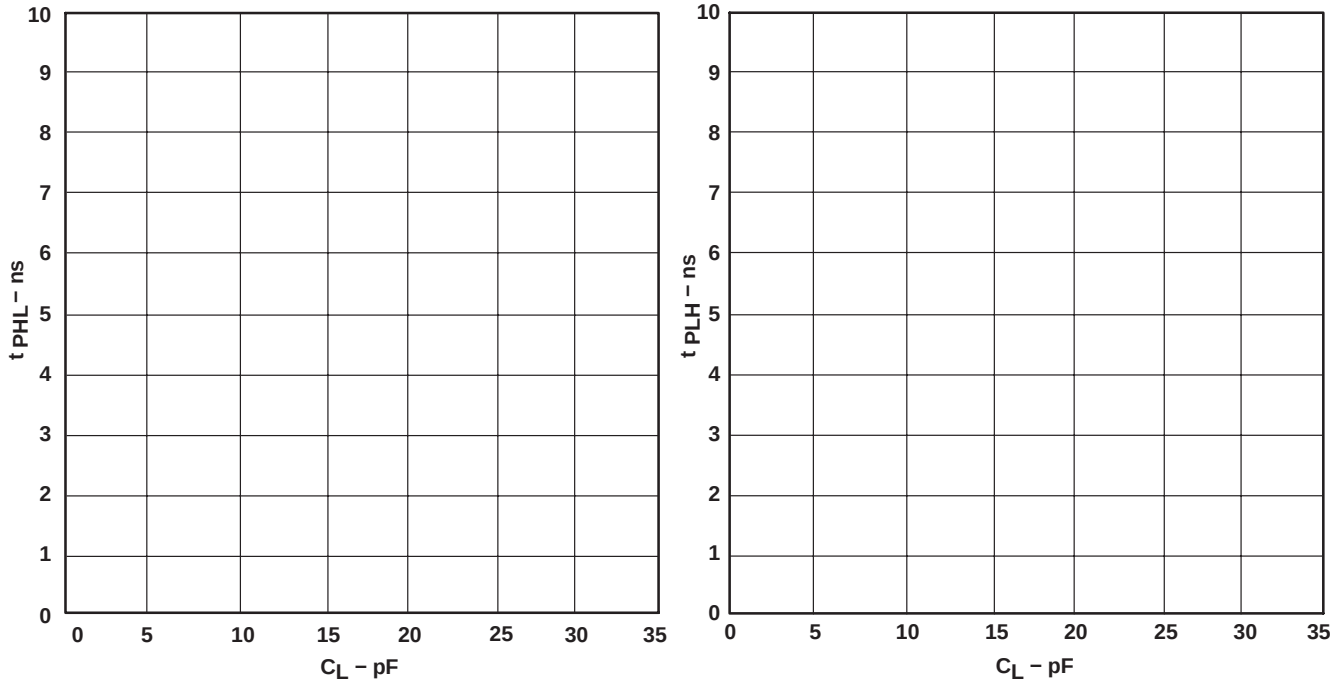
PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

TYPICAL PROPAGATION DELAY (A TO B) vs LOAD CAPACITANCE
$T_A = 25°C$, $V_{CCA} = 2.5$ V

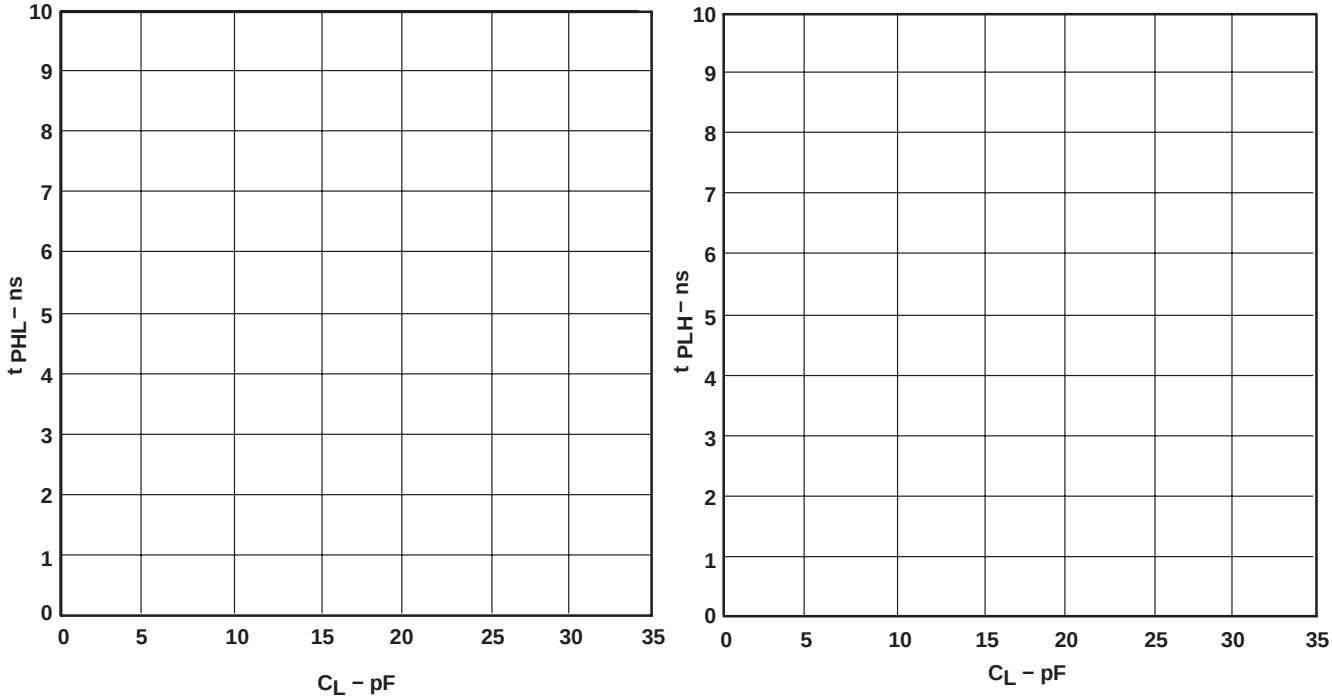


TYPICAL PROPAGATION DELAY (B TO A) vs LOAD CAPACITANCE
$T_A = 25°C$, $V_{CCA} = 2.5$ V

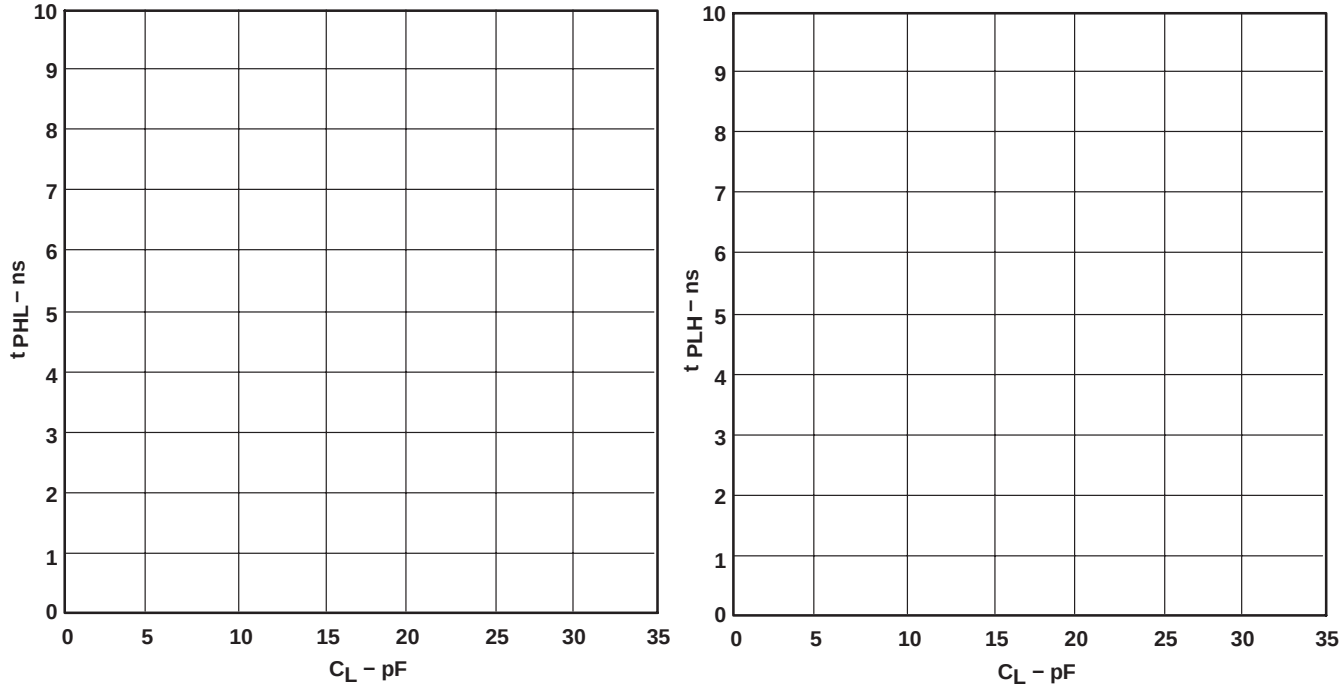


TYPICAL CHARACTERISTICS

TYPICAL PROPAGATION DELAY (A TO B) vs LOAD CAPACITANCE
$T_A = 25°C$, $V_{CCA} = 3.3$ V



TYPICAL PROPAGATION DELAY (B TO A) vs LOAD CAPACITANCE
$T_A = 25°C$, $V_{CCA} = 3.3$ V

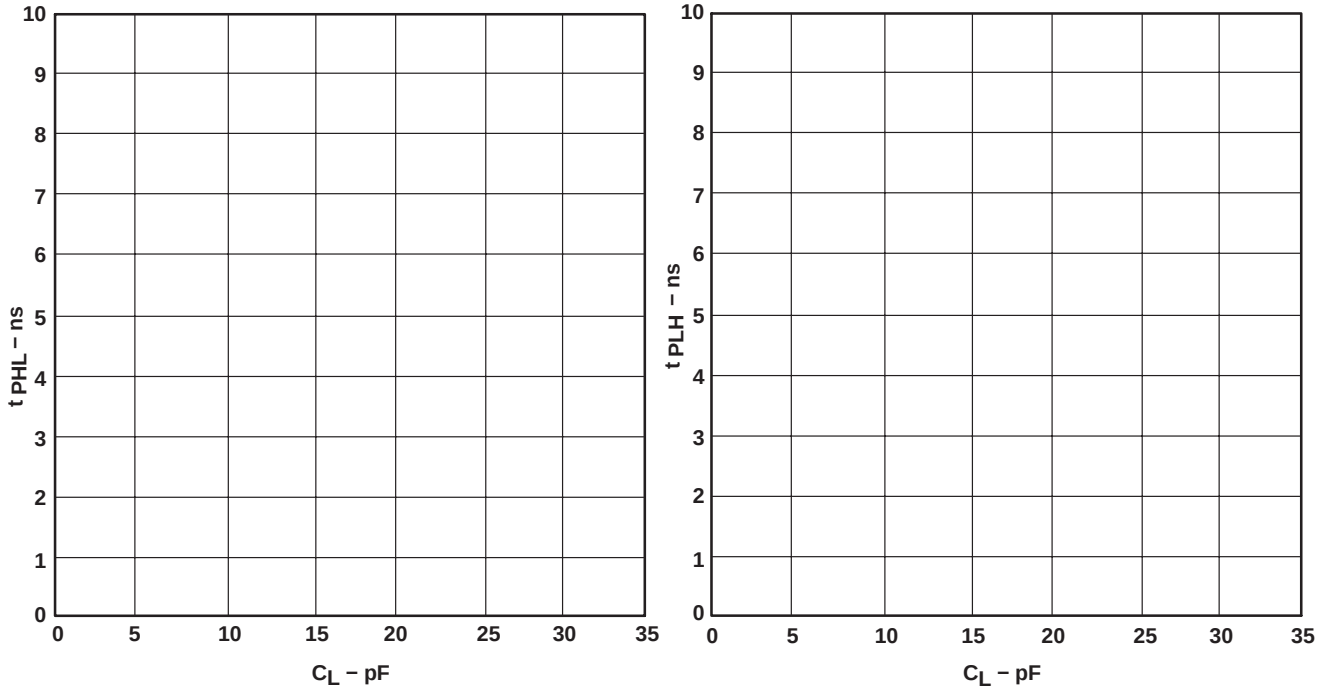


PRODUCT PREVIEW

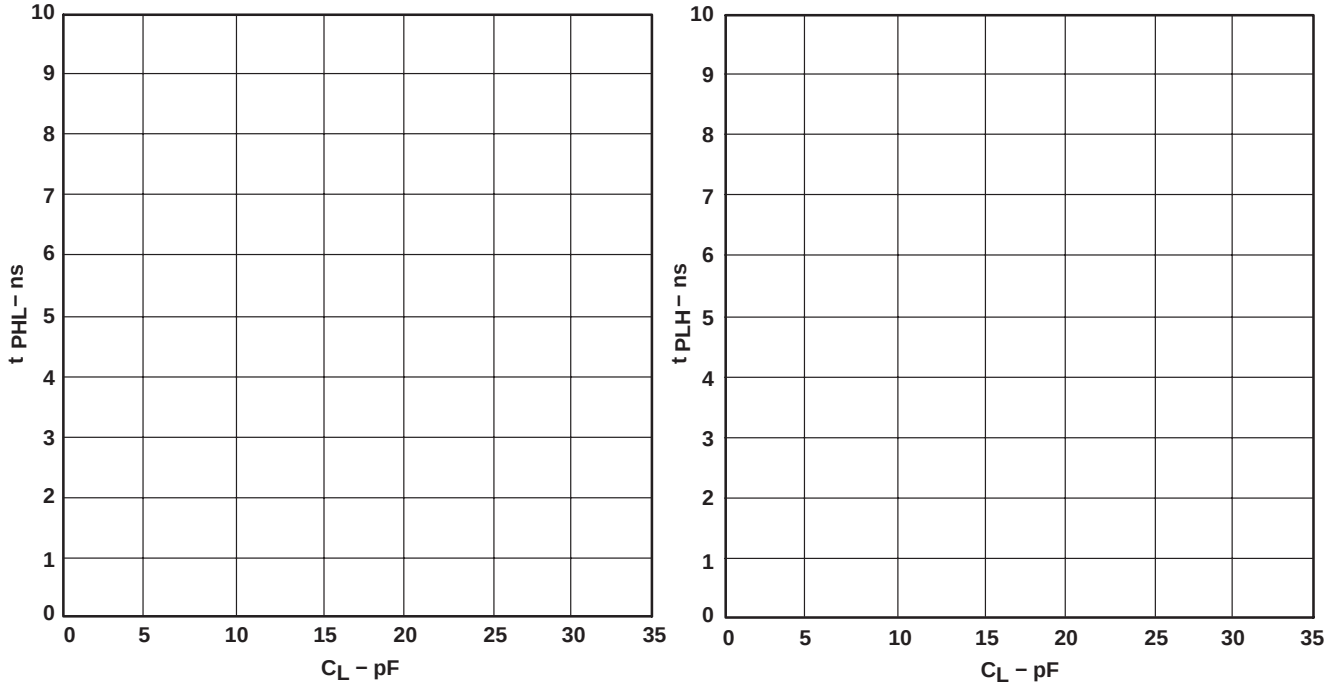
PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

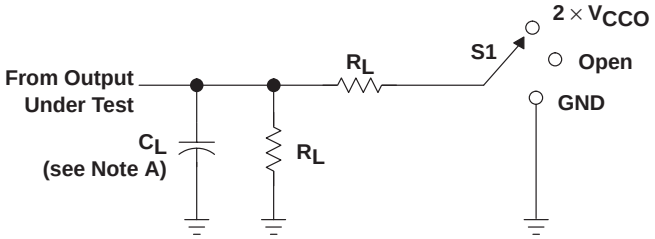
TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
$T_A = 25°C$, $V_{CCA} = 5$ V



TYPICAL PROPAGATION DELAY (B TO A) vs LOAD CAPACITANCE
$T_A = 25°C$, $V_{CCA} = 5$ V



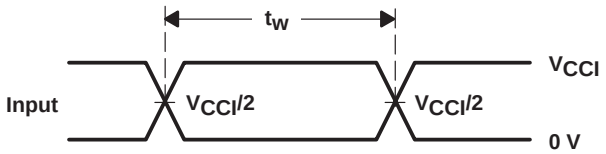
PARAMETER MEASUREMENT INFORMATION



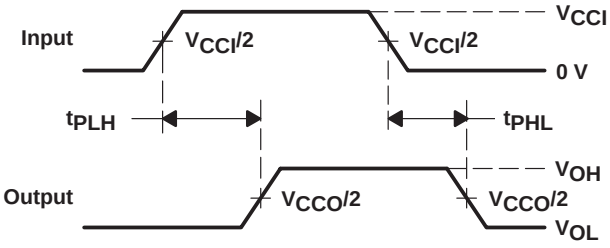
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

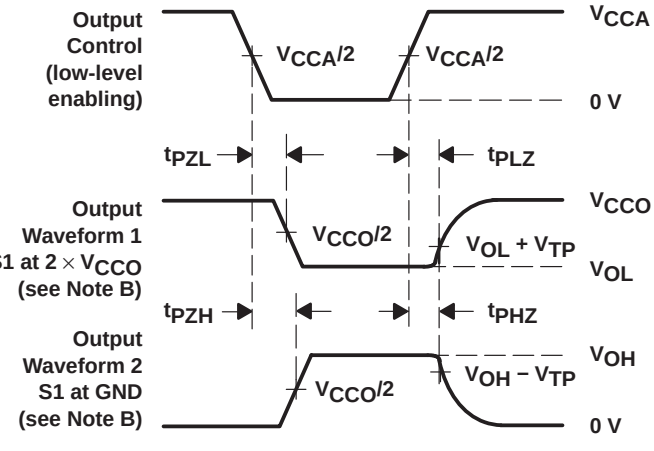
V_{CCO}	C_L	R_L	V_{TP}
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V
5 V ± 0.5 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



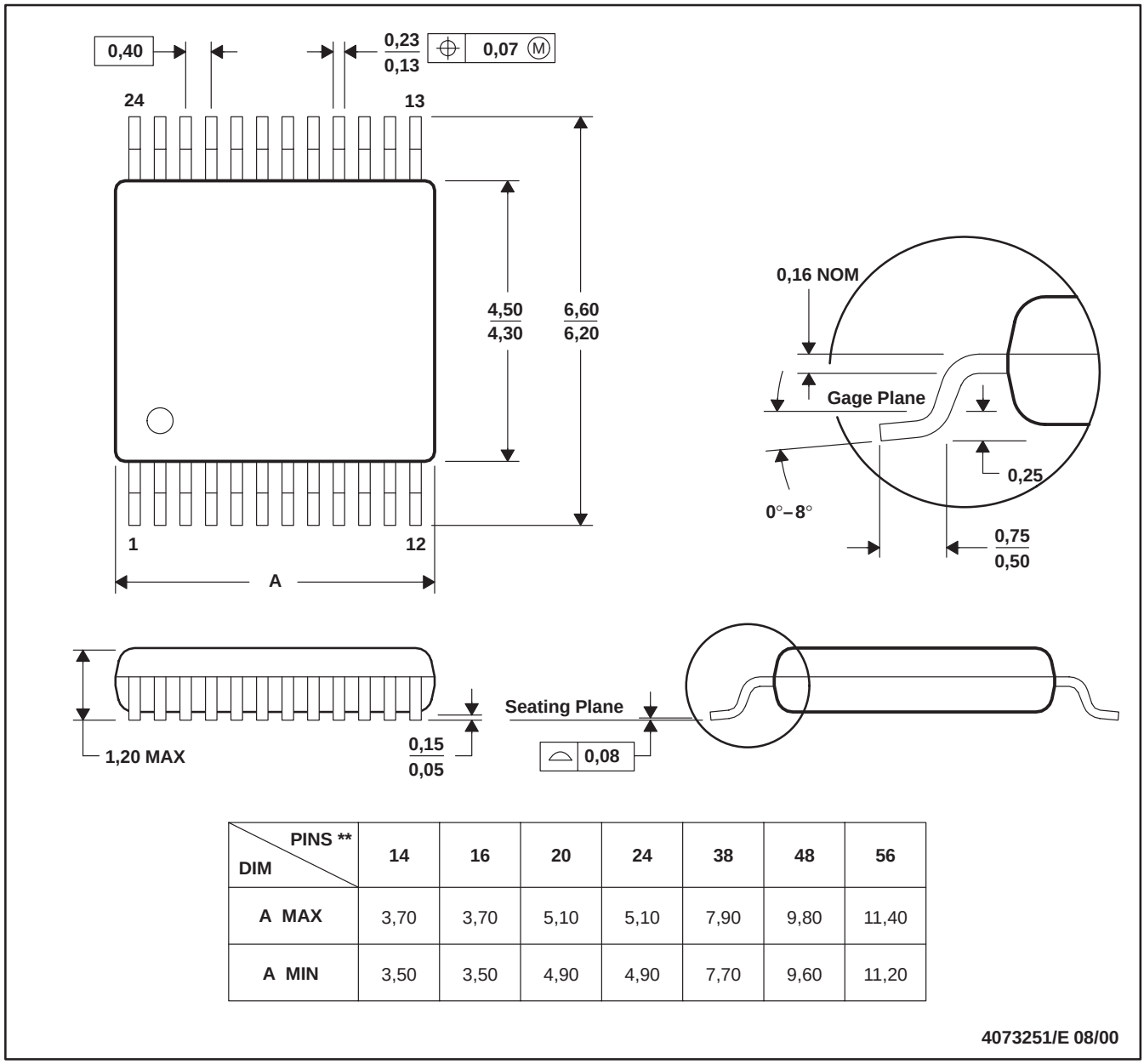
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns, dv/dt ≥1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.
J. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

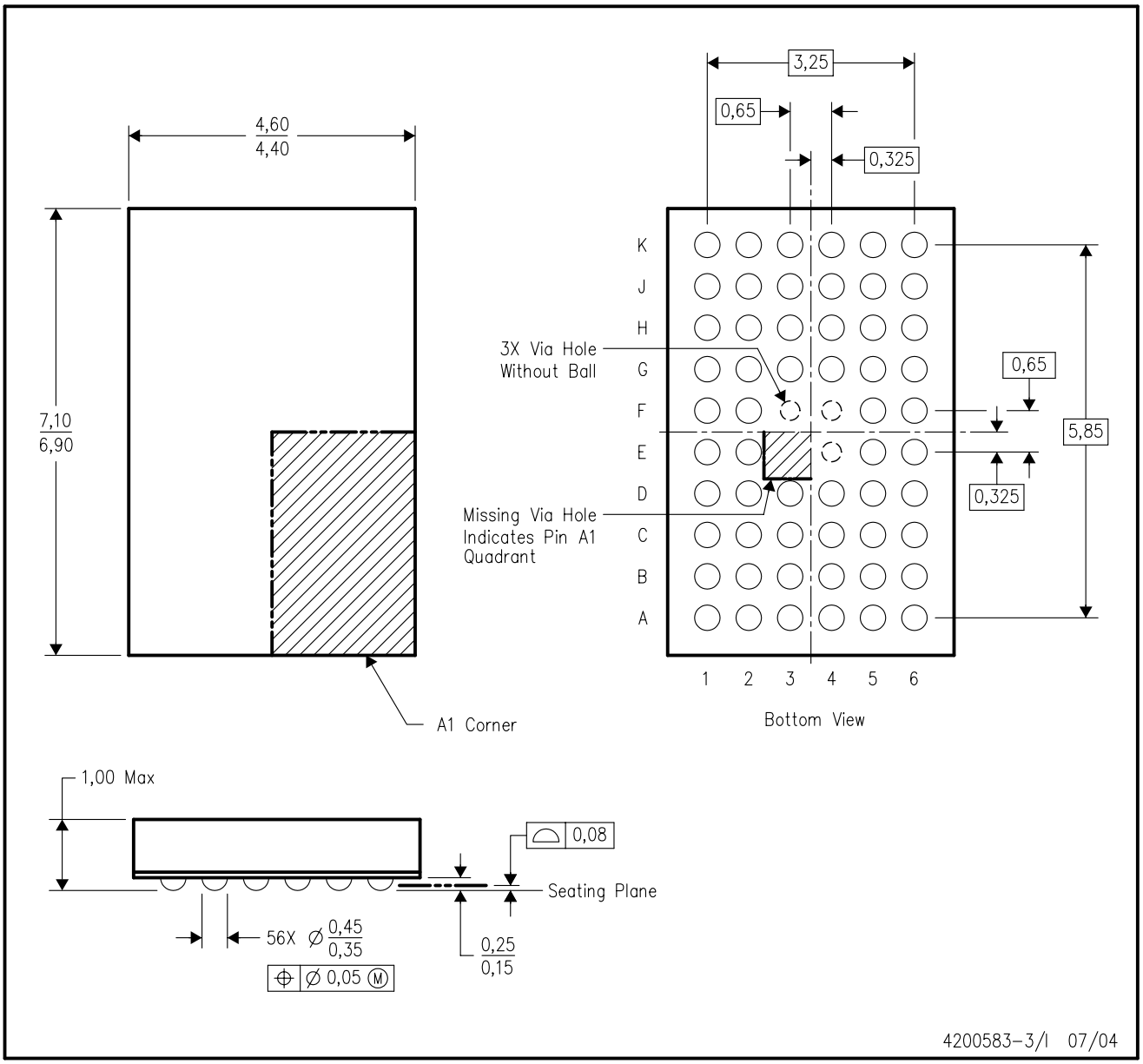


DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

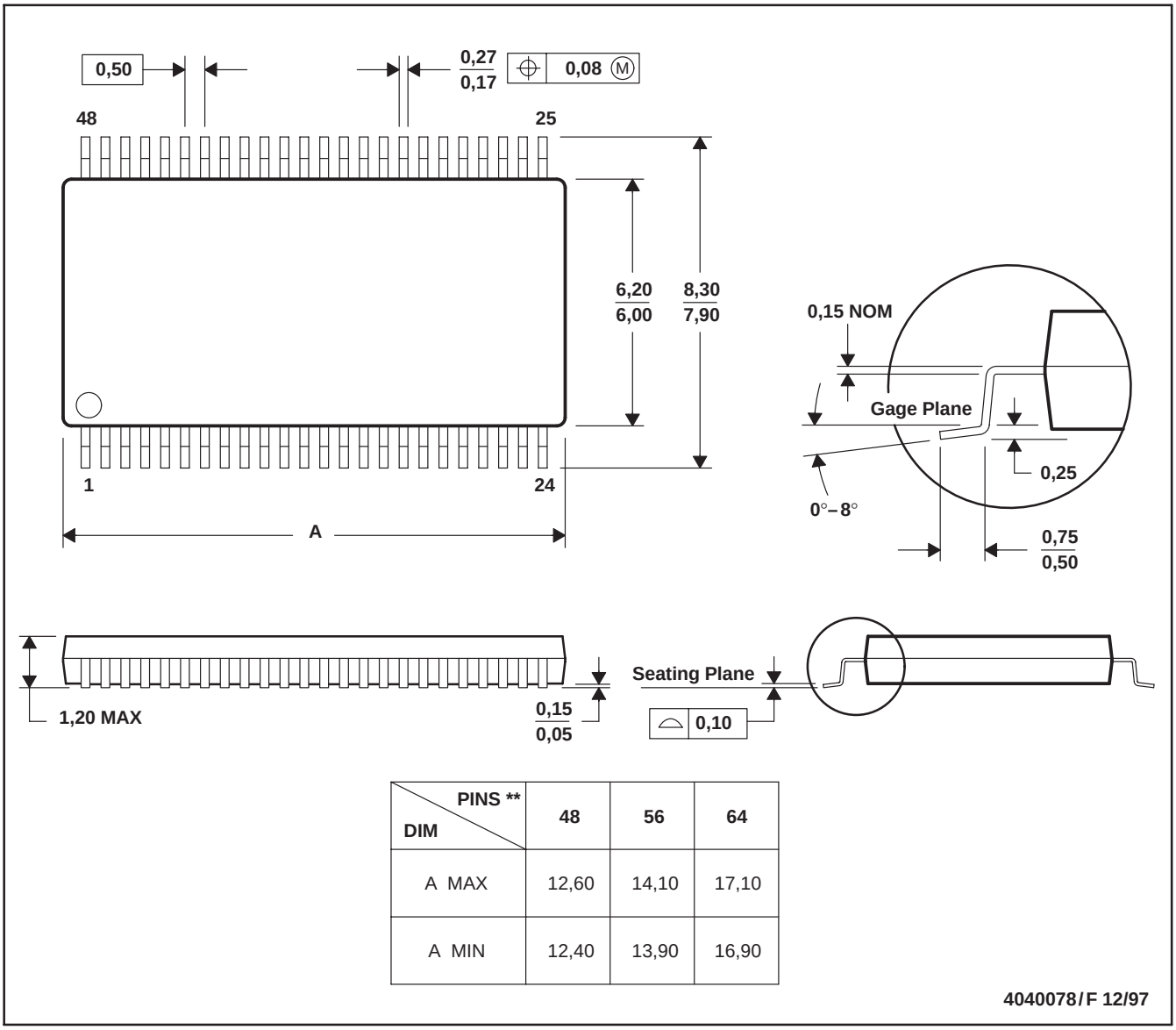
GQL (R–PBGA–N56) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225 variation BA.
D. This package is tin–lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead–free.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265