AS3605
Multi-Standard Power Management Unit

1 General Description

The AS3605 is a highly-integrated CMOS power management device designed specifically for portable devices such as mobile phones, PDAs, CD players, digital cameras and other devices powered by 1-cell Li-Ion battery. It can be used for any mobile phone handset standards such as CDMA, WCDMA, GSM, GPRS, EDGE, UTMS and other Japanese or American standards.

The device incorporates low dropout regulators (LDOs), a DC/DC converter, a complete battery charger, and an audio power amplifier on one die.

The linear analog LDOs feature extremely high performance regarding:

- Noise – typ 30µV$_{RMS}$ from 100Hz to 100kHz
- Line/Load Regulation – < 1mV static, < 10mV transient
- Power Supply Rejection – > 70dB @ 1kHz

The integrated Step Down DC/DC Converter does not require an external Schottky diode yet provides very high efficiency (up to 95%) throughout the whole operating range.

5 programmable current sources are included to control LED brightness.

A low-distortion audio power amplifier (1 Watt @ 8Ω) supports handsfree operation and HiFi ring-tones.

The device also features a battery charger including automatic trickle charging, and programmable constant voltage and current charging.

The AS3605 is controlled via a serial interface and integrates all necessary system specific functions such as Reset, Watchdog, and Power-On Detection.

Output voltages and start-up timings can be programmed via the internal OTP.

2 Key Features

- 8 Programmable High Performance LDOs
    - Four RF Low-Noise LDOs (1.8 to 3.35V, 150mA)
    - Two Analog Low-Noise LDOs (1.8 to 3.35V, 250mA)
    - One SIM Low-Power LDO (1.8 or 3.0V, 20mA)
    - One Low-Power LDO (2.5V, 10mA)
- Programmable High Efficiency DC/DC Converter
    - Step Down: 0.6 to 3.4V, up to 500mA with 2.2MHz
- Stereo Audio Power Amplifier
    - 0.5W @ 4Ω – Stereo; 1W @ 8Ω – Bridged
    - Digital Volume Control, 3dB Steps
    - Click- and Pop-Less Start-Up and Power-Down

- Battery Charger
    - Automatic Trickle Charging
    - Programmable Constant Current Charging
    - Programmable Constant Voltage Charging
    - Safety Functions (Low Battery Shutdown)
    - Over- and Under-Temperature Charge Disable
    - Operation without Battery
    - Can Regulate the Current Through the Battery or from the Charger
    - Charger Input Overvoltage Protection (6V)
    - Shutdown even with Connected Charger
    - Charger Resume Operation
    - Charger Interrupts (Inserted, Removed, Overvoltage, Resume)
    - No-Battery Detection
- Momentary Power Loss Detection
    - Battery Supply Short-Interruption Detection (<200ms); (e.g., due to a dropped phone)
- Five Programmable Current Sources (3x40mA, 2x160mA)
    - 8-Bit (0.625 to 160mA)
    - Buzzer, Vibrator, LEDs
- Charge Pump (1:1 and 1:2 mode) 60mA @3.3V VBAT
- OTP programmable boot sequence
- Wide Battery Supply Range 3.0 to 5.5V
- Three Programmable General Purpose I/O Pins
- On-Chip Bandgap Tuning for High Accuracy (±1%)
- Integrated Programmable Watchdog (16 to 4080ms)
- Programmable Reset (0 to 70ms)
- Shutdown Current typ <10µA (2.5V Always On)
- Overcurrent and Thermal Protection
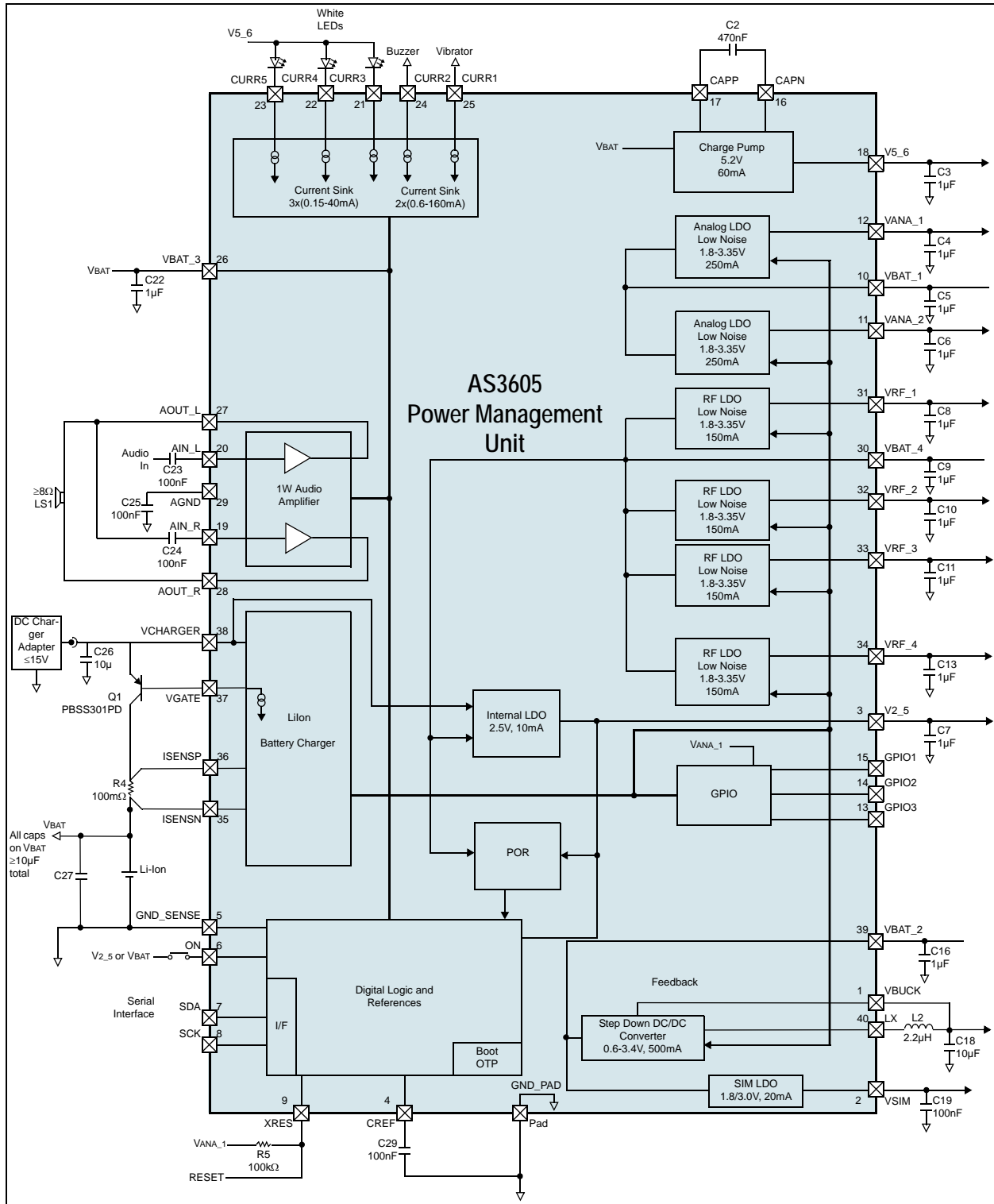- 1.5 Watt Power Dissipation @T$_A$ = 70ºC

### Packaging
QFN40 5x5mm, 0.4mm pitch

3 Application

Multi-standard power management for mobile phones, PDAs, and any other 1-cell Li+ powered devices.

Figure 1. *AS3605 Block Diagram. Option: Audio Amplifier In Differential Mode, Step Down DC/DC Converter as Pre-Regulator for Digital LDOs*

Note: Refer to Table 33 for specifications of external components.

Figure 2.   AS3605 Block Diagram. Option: Audio Amplifier in Stereo Single-Ended Mode, Digital LDOs Separated from Step Down DC/DC Converter
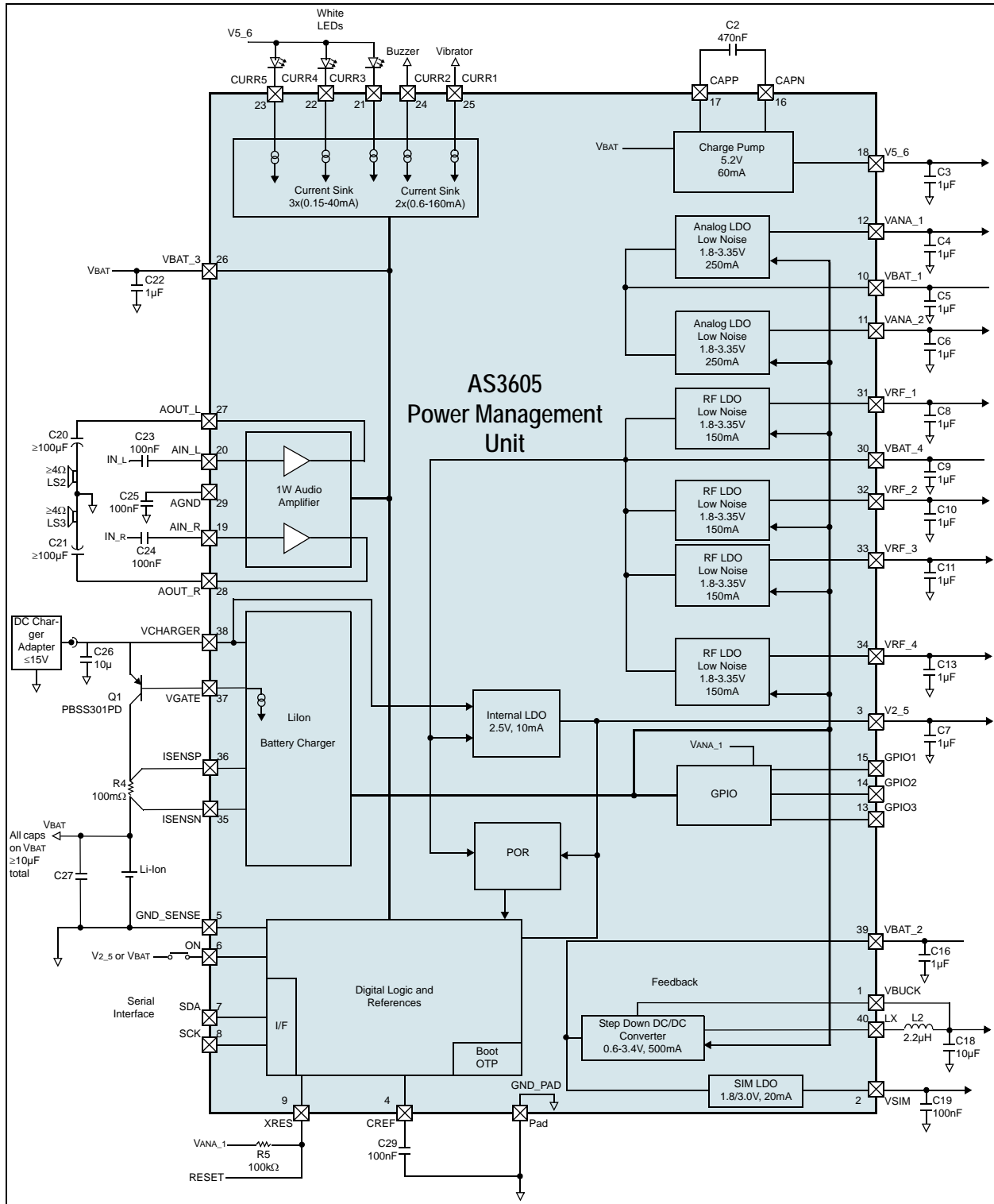
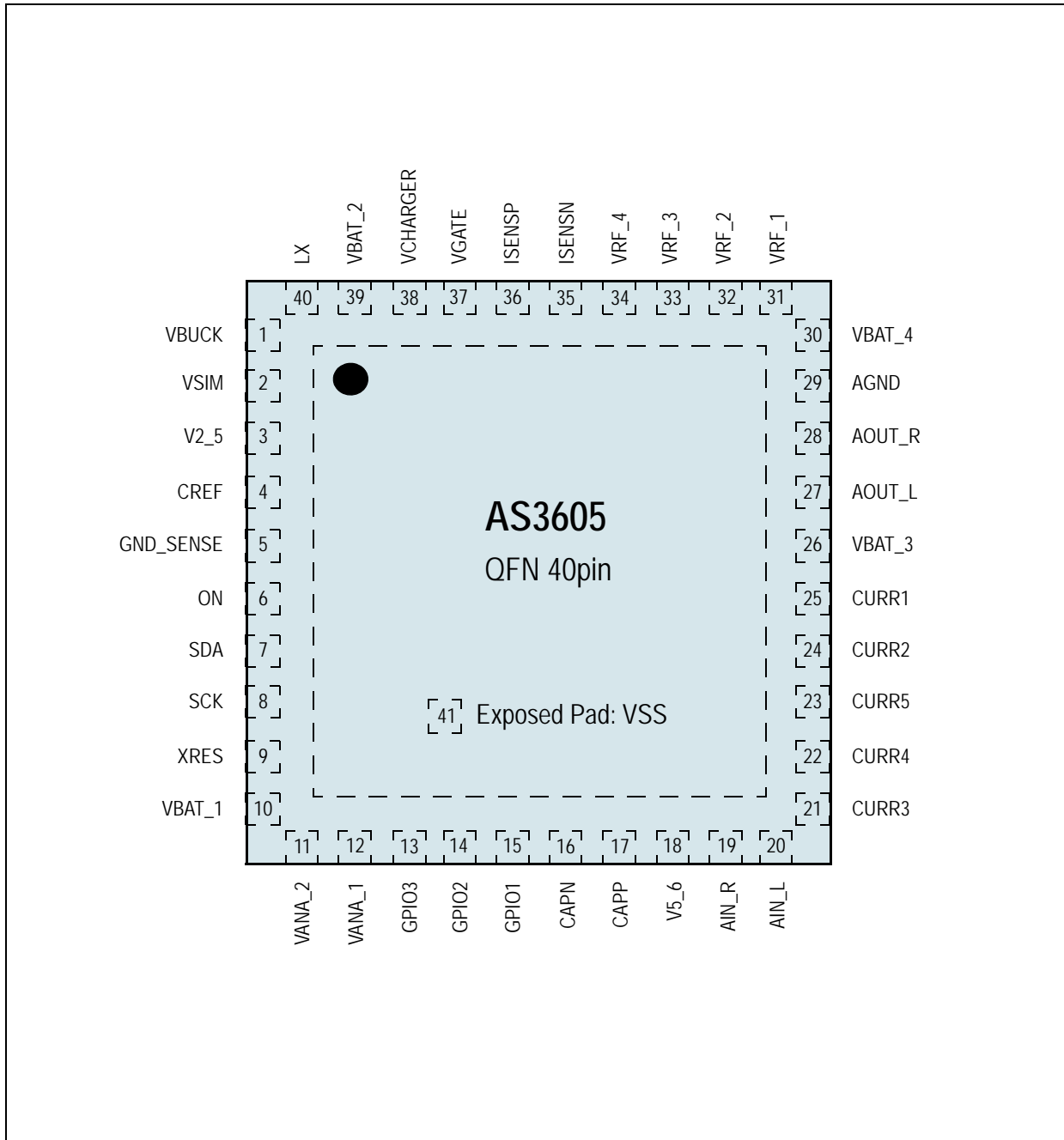**Note:**   Refer to Table 33 for specifications of external components.

Contents

4 Pin Assignments

Figure 3. Pin Assignments (Top View)

4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
VBUCK	1	Analog Input	Sense input of the DC/DC converter.
VSIM	2	Analog Output	Output voltage of LDO VSIM; if used, connect a ceramic capacitor of 100nF (±20%).
V2_5	3	Analog Output	Output voltage of low power LDO V2_5; always connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100% / -50%); do not load this pin during startup.
CREF	4	Analog Pin	Bypass capacitor for the internal voltage reference; always connect a capacitor of 100nF. **Caution:** Do not load this pin.
GND_SENSE	5	Analog Pin	Sensitive GND for Bandgap Voltage Reference.
ON	6	Digital Input	Input pin to startup the AS3605 (power on); internal pulldown; sense output in test mode.
SDA	7	Digital Input	SDA input/output in I^2C mode.
SCK	8	Digital Input	SCK input in I^2C mode.
XRES	9	Digital Input/Output / Open Drain (device can only pulldown this pin)	Bidirectional active low RESET pin; add an external pullup resistor.
VBAT_1	10	Supply Pin	Supply pin for Analog LDOs VANA_1 and VANA_2 as well as the charge pump; can be connected to V$_{BAT}$ or separate supply (3.0-5.5V).
VANA_2	11	Analog Output	Output voltage of one of Analog LDO VANA_2; if used as LDO, connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100% / -50%).
VANA_1	12	Analog Pin	Output voltage of Analog LDO VANA_1; if used as LDO, connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100% / -50%).
GPIO3	13	Digital Input/Output	General purpose switchable 5V input/output.
GPIO2	14	Digital Input/Output	General purpose switchable 5V input/output.
GPIO1	15	Digital Input/Output	General purpose switchable 5V input/output.
CAPN	16	Analog Pin	Flying capacitor of the Charge Pump; if used connect a ceramic capacitor of 470nF (±20%) to this pin.
CAPP	17	Analog Pin	Flying capacitor of the Charge Pump; if used, connect a ceramic capacitor of 470nF (±20%) to this pin.
V5_6	18	Analog Pin	Output voltage of the Charge Pump; if used, connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100% / -50%).
AIN_R	19	Analog Input	Audio Amplifier right-channel input.
AIN_L	20	Analog Input	Audio Amplifier left-channel input; sense output in test mode.
CURR3	21	Analog Input	Analog current sink input.
CURR4	22	Analog Input	Analog current sink input.
CURR5	23	Analog Input	Analog current sink input.
CURR2	24	Analog Input	Analog current sink input.
CURR1	25	Analog Input	Analog current sink input.
VBAT_3	26	Supply Pin	Supply pin for Current Sinks, and Audio Amplifier; always connect to V$_{BAT}$.
AOUT_L	27	Analog Output	Audio Amplifier left-channel output.
AOUT_R	28	Analog Output	Audio Amplifier right-channel output.

Table 1. Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
AGND	29	Analog Pin	Audio Amplifier reference GND; if the Audio Amplifier is used, connect a capacitor of 100nF (±10%) to this pin. **Caution:** Do not connect directly to VSS.
VBAT_4	30	Supply Pin	Supply pad for RF-LDOs VRF_1, VRF_2, VRF_3 and VRF_4; can be connected to V$_{BAT}$ or separate supply (3.0-5.5V).
VRF_1	31	Analog Output	Output voltage of RF LDO VRF_1; if used, connect a ceramic capacitor of 1μF (±20%) or 2.2μF (+100% / -50%).
VRF_2	32	Analog Output	Output voltage of RF LDO VRF_2; if used, connect a ceramic capacitor of 1μF (±20%) or 2.2μF (+100% / -50%).
VRF_3	33	Analog Output	Output voltage of RF LDO VRF_3; if used, connect a ceramic capacitor of 1μF (±20%) or 2.2μF (+100% / -50%).
VRF_4	34	Analog Output	Output voltage of RF LDO VRF_4; if used, connect a ceramic capacitor of 1μF (±20%) or 2.2μF (+100% / -50%).
ISENSN	35	Analog Input	Negative sensing input voltage for the external charging current shunt resistor.
ISENSP	36	Analog Input	Positive sensing input voltage for the external charging current shunt resistor.
VGATE	37	Analog Output	Control pin for the external battery charger MOSFET transistor.
VCHARGER	38	Analog Input	High voltage input coming from the Battery Charger; if the Battery Charger is used, connect a ceramic capacitor of 1μF.
VBAT_2	39	Supply Pin	Supply pin for the Step Down DC/DC Converter and LDO VSIM; always connect to V$_{BAT}$.
LX	40	Analog Output	Step Down DC/DC Converter switch output to coil
VSS	41	V$_{SS}$	Ground pad (QFN40: exposed paddle).

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Operating Conditions on page 10 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Comments
V_{IN_HV}	High Voltage Pins	-0.3	18.0	V	Applicable for high voltage pins: VCHARGER, VGATE
V_{IN_MV}	5V Pins	-0.3	7.0	V	Applicable for pins 5V pins: VBAT_1 - VBAT_4, V5_6, VBUCK, GPIO1 - GPIO3, CURR1 - CURR5, VANA_1, VANA_2, AIN_L, AIN_R, AOUT_L, AOUT_R, XRES, SCK, SDA, ON, and LX
V_{IN_LV}	3.3V Pins	-0.3	5.0	V	Applicable for 3.3V pins: VRF_1 - VRF_4, VSIM, CAPN, AGND, ISENSP, ISENSN, V2_5, CREF
I_{IN}	Input Pin Current	-25	+25	mA	At 25ºC Norm: JEDEC JESD78C
	Humidity	5	85	%	Non-condensing
Continuous Power Dissipation (T_A = +70ºC)					
P_T	Continuous power dissipation		1.5	W	P_T[1] for QFN40 package
Electrostatic Discharge					
V_{ESD}	Electrostatic Discharge HBM		±1.5	kV	Norm: JEDEC JESD22-A114F
Temperature Ranges and Storage Conditions					
T_j	Junction Temperature		+110	ºC	
T_{strg}	Storage Temperature Range	-55	+125	ºC	
	Humidity non-condensing	5	85	%	
Temperature (soldering)					
	Package Body Temperature		260	ºC	Norm IPC/JEDEC J-STD-020[2], reflects moisture sensitivity level only
	Moisture Sensitive Level	3			Represents a maximum floor live time of 168h

1. Depending on actual PCB layout and PCB used.

2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

6 Electrical Characteristics

Table 3. Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
T_{AMB}	Ambient Temperature	-40	25	85	ºC	
V_{HV}	High Voltage	0.0		15.0	V	Pins VCHARGER, VGATE
V_{BAT}	Battery Voltage	3.0	3.6	5.5	V	For pins VBAT_1 - VBAT_4. During startup from external battery charger adapter, the battery voltage can be below 3.0V.
V_{ANA_1}	Periphery Supply Voltage for GPIO pins	1.8	OTP	3.35	V	Internally generated from V_{ANA_1}
V_{ON}	Activation voltage for ON pin	1.75	V_{2_5}	V_{BAT}	V	
V_{2_5}	Voltage on Pin V2_5	2.4	2.5	2.6	V	Internally generated
V_{5_6}	Output Voltage of Charge Pump	4.9	5.2	5.6	V	2 x VBAT_1
I_{BAT}	Operating Current		195	260	µA	Normal operating current. With bit **low_power_on** = 0; only V_{ANA_1} active, no additional external loads.
$I_{LOWPOWER}$	Low-Power Mode Current Consumption		110		µA	With bit **low_power_on** = 1; only V_{ANA_1} active, no additional external loads.
$I_{POWEROFF}$	Power-Off Mode Current Consumption		10	20	µA	With bit **power_off** = 1; only V2_5 is active in power OFF mode. Not tested, guaranteed by design

7 Detailed Description

7.1 Battery Charge Controller

The AS3605 device serves as a standalone battery charge controller supporting rechargeable lithium ion (Li+) and) batteries. Requiring only a few external components, a full-featured battery charger with a high degree of flexibility can easily be realized. The main features of the controller are:

- Charge adapter detection
- Internal voltage regulator
- Low current (trickle) charging
- Constant current charging
- Constant voltage charging
- Overvoltage protection
- Battery presence indication
- Operation without battery

Figure 4. Charger Application Block Diagram
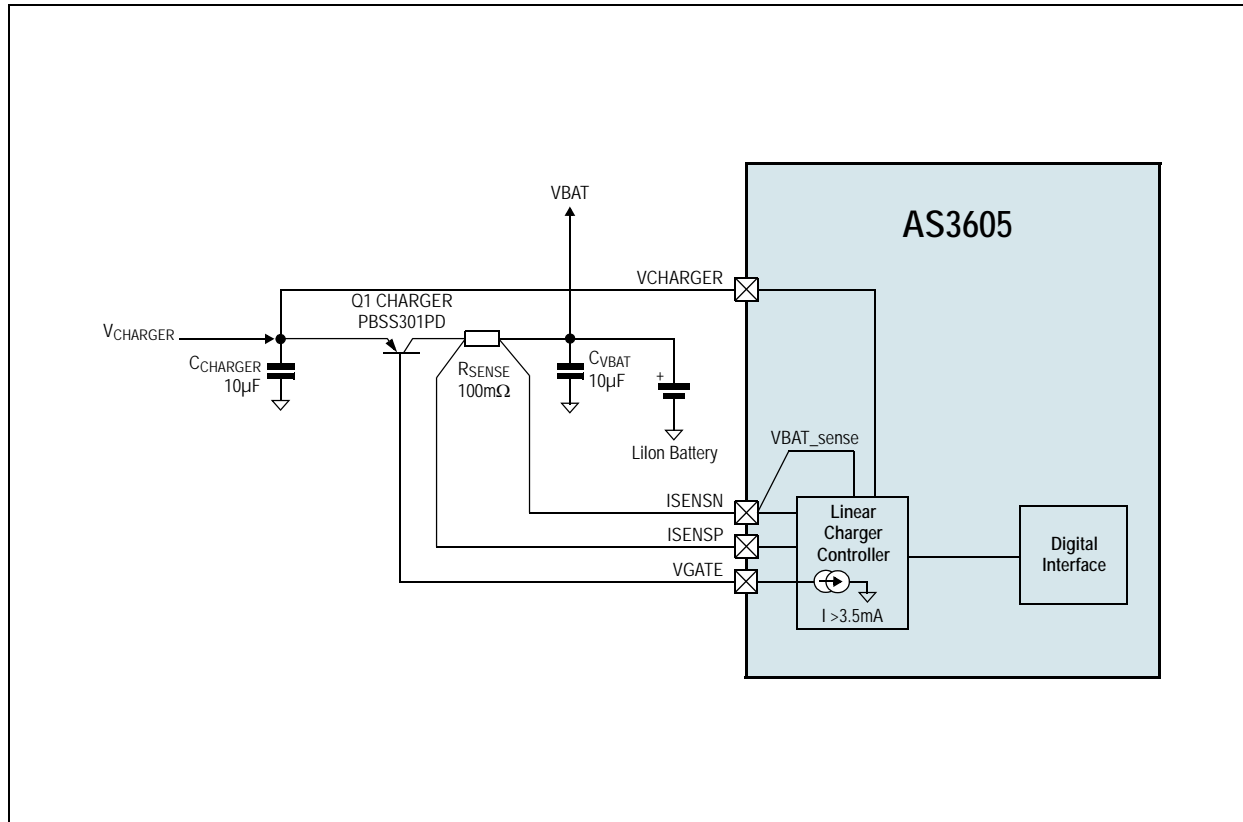
Table 4. Charger External Components

Symbol	Component	Value	Note
Q_1	PNP power transistor	PBSS301PD or similar	$h_{FE} > 200$ @ 0.8A
R_{SENSE}	Current sense resistor	100mΩ ±1%, 125mW for $I_{CHG} < 1.5$A	e.g. Vishay Dale WSL0805
C_{CHRG}	Bypass capacitor on charger pin	10µF ±20%, X5R or X7R dielectric	
C_{BAT}	Minimum total capacitance parallel to battery	10µF, X5R or X7R dielectric	

7.1.1   Charge Controller Operating Modes and Building Blocks

Charge Adapter Detection. The charge controller uses an integrated detection circuit to determine if an external charge adapter has been applied to the VCHARGER pin. If the adapter voltage exceeds the battery voltage at pin VBAT by VCHDET the **ChDet** bit in the **ChargerStatus** register will be set. The detection circuit will reset the charge controller (bit **ChDet** is cleared) as soon as the voltage at the VCHARGER pin drops to only VCHMIN above the battery voltage. In case the AS3605 device is reset the charge controller will also be reset, even if a charge adapter is applied to the VCHARGER pin.

Low Current (trickle) Charging. Trickle charge mode is started when an external charge adapter has been detected and the battery voltage at pin VBAT is below the VUVLO threshold; bits **ChAct** and **Trickle** will be set in the **ChargerStatus** register. In this mode the charge current will be limited to **TrickleCurrent[1:0]** (set in the **ChargerControl1** register) to prevent undue stress on either the battery or any of the charger components in case of deeply discharged batteries. Once VUVLO has been exceeded, the charger will change over to constant current charging (**Trickle** is cleared) and switch on the device.

Constant Current Charging. Constant current charging is initiated by setting **ChEn** in the **ChargerControl1** register. Note that **ChEn** is set by default to enable operation of the device without a battery connected to the system. The **ChAct** bit is set when the charger has started, and the charge current will be limited to **ConstantCurrent[3:0]** (set in the **ChargerControl1** register) by the battery charge controller. When the battery approaches full charge, its voltage will exceed the charge termination threshold VCHOFF. VCHOFF depends on the **Li4v2** bit in the **ChargerControl2** register. The charging action will either be terminated (**EOC** bit will be set) or a top-off charge will be started (**CVM** will be set).

Constant Voltage Charging. Constant voltage charge mode is initiated and the **CVM** bit will be set when the VCHOFF threshold has been reached.
The charge current is monitored during constant voltage charging. It will be decreasing from its initial value during constant current charging and eventually drop below the value set by **TrickleCurrent[1:0]** in the **ChargerControl1** register. If the measured charge current is less than or equal to **TrickleCurrent[1:0]**, the charging cycle is terminated and **EOC** is set.

Battery Presence Indication and Operation Without Battery. After EOC state is reached a timer for NOBAT detection is started. If there is no battery present, the voltage will drop to V_{NOBAT_REG}. Depending on the load on VBAT and the capacitor on VBAT this might take some mseconds to 1 second. If the RESUME mode is enabled (Bit **resume_disable**=0), the charger will restart charging (ConstantCurrent charging) after 100msec.
The 100msec dead time is necessary to get a battery oscillation frequency of below 10Hz, if there is no battery present.
If the NOBAT detection timer is below 2 seconds after reaching EOC state, and this happens 2 times in serial, the NOBAT bit in **ChargerStatus** register is set. If a battery is inserted, then the bit will be reset after the timer exceeds the 2 seconds.

Charger Overvoltage Protection. This blocks checks if the charger voltage is above 6.05V or 6.45V if **ChOvH** is 1. If the status bit **ChOv** is 1 when **ChOvEn** is 1, the charger will shut down by clearing the **ChEn** bit and an interrupt will be generated.

Table 5. Charger Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VCHDET	Charger detection threshold	50	75	105	mV	Hysteresis is > 40mV
VCHMIN		0	20	35		
VCHOVH	VCHARGER overvoltage detection	6.2	6.45	6.71	V	**ChOvH** = 1
		5.81	6.05	6.29		**ChOvH** = 0
VUVLO	Undervoltage lockout threshold		3.1		V	VBAT rising
			2.8			VBAT falling
VCHOFF	Charge termination threshold	4.158	4.20	4.242	V	Li+ Battery: **Li4v2** = 1
			4.10			Li+ Battery: **Li4v2** = 0
VNOBATREG	"No battery" regulation voltage		3.85		V	Li+ Battery: **Li4v2** = 1
			3.75			Li+ Battery: **Li4v2** = 0
VRESUME_ON	Charger resume on threshold		3.85		V	**Li4v2** = 1
			3.75			**Li4v2** = 0

Table 5. Charger Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{RESUME_OFF}	Charger resume off threshold		4.02		V	**Li4v2** = 1
			3.92			**Li4v2** = 0
I_{GATE_OFF}	Current into pin GATE, if charger disabled	0		0.4	µA	VCHARGER=5V
I_{GATE_ON}	Current into pin GATE, if charger enabled and operation in low dropout mode (low V_{CE})	3.5	5		mA	VCHARGER=5V

7.1.2   Charger Registers

Table 6. Charger Register Summary

Name	Addr.	b7	b6	b5	b4	b3	b2	b1	b0	Page
LDO_CHG	10h					EOCCurrent[1:0]				14
ChargerControl1	14h	ChOvEn	TrickleCurrent[1:0]		ConstantCurrent[3:0]				ChEn	13
ChargerControl2	16h	ChOv	ChOvH	NA	Li4v2	resume_disable				14
ChargerStatus	35h	NA	NoBat	EOC	CVM	Trickle	NA	ChAct	ChDet	15

ChargerControl1 Register (Address 14h).

Addr: 14h		ChargerControl1				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**		
0	ChEn	1b	R/W	0	Disable charging	
				1	Enable charging	
4:1	ConstantCurrent[3:0]	OTP	R/W	0	0mA + Trickle_current	
				1	50mA + Trickle_current	
				2	100mA + Trickle_current	
				3	150mA + Trickle_current	
				4	200mA + Trickle_current	
				5	250mA + Trickle_current	
				6	300mA + Trickle_current	
				7	350mA + Trickle_current	
				8	400mA + Trickle_current	
				9	450mA + Trickle_current	
				A	500mA + Trickle_current	
				B	550mA + Trickle_current	
				C	600mA + Trickle_current	
				D	650mA + Trickle_current	
				E	700mA + Trickle_current	
				F	750mA + Trickle_current	

Addr: 14h		ChargerControl1				
Bit	Bit Name	Default	Access	Bit Description		
6:5	TrickleCurrent[1:0]	OPT	R/W	0	50mA	
				1	100mA	
				2	150mA	
				3	200 mA	
7	ChOvEn	1	R/W	0	Disable the Charger Overvoltage protection	
				1	Enable the Charger Overvoltage protection	

LDO_CHG Register (Address 10h).

Addr: 10h		LDO_CHG				
		Adjusts EOC current of Charger.				
Bit	Bit Name	Default	Access	Bit Description		
3:2	EOCCurrent[1:0]	00	R/W	00	EOC Current = Trickle Current	
				01	EOC Current = Trickle Current + 18mA	
				10	do not use	
				11	EOC Current = Trickle Current + 33mA	

ChargerControl2 Register (Address 16h).

Addr: 16h		ChargerControl2				
Bit	Bit Name	Default	Access	Bit Description		
2:0	-	NA	NA			
3	resume_disable	0	R/W	0	Enable Resume in **EOC** state	
				1	Disable Resume in **EOC** state	
4	Li4v2	1	R/W	0	V_{CHOFF} = 4.1V for Li+ battery cells with coke anode	
				1	V_{CHOFF} = 4.2V for Li+ battery cells with graphite anode	
5	-	NA	NA			
6	ChOvH	1	R/W	0	Sets low threshold for Over voltage protection (typ. 6.05V)	
				1	Sets high threshold for Over voltage protection (typ. 6.45V)	
7	ChOv	NA	R	Indicates Charger overvoltage condition		

ChargerStatus Register (Address 35h).

Addr: 35h		ChargerStatus		
		Read only		
Bit	Bit Name	Default	Access	Bit Description
0	ChDet	NA	R	Bit is set when external charge adapter has been detected
1	ChAct	NA	R	Bit is set when charger is operating
2	-	NA		
3	Trickle	NA	R	Bit is set when charger is in trickle charge mode
4	CVM	NA	R	Bit is set when charger is in top-off charge mode
5	EOC	NA	R	Bit is set when charging has been terminated. Bit is cleared automatically when **ChEn** is cleared.
6	NoBat	NA	R	Bit is set when battery detection circuit indicates that no battery is connected to the system. Bit is cleared automatically when a battery is connected or when **ChEn** is cleared.
7	-	NA	NA	

7.2 Step Down DC/DC Converter

The step-down converter is a high-efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches, efficiency up to 95% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 500mA, with an output capacitor of only 10µF. The implemented current limitation protects the DC/DC Converter and the coil during overload condition.

Figure 5. Step Down DC/DC Converter Block Diagram
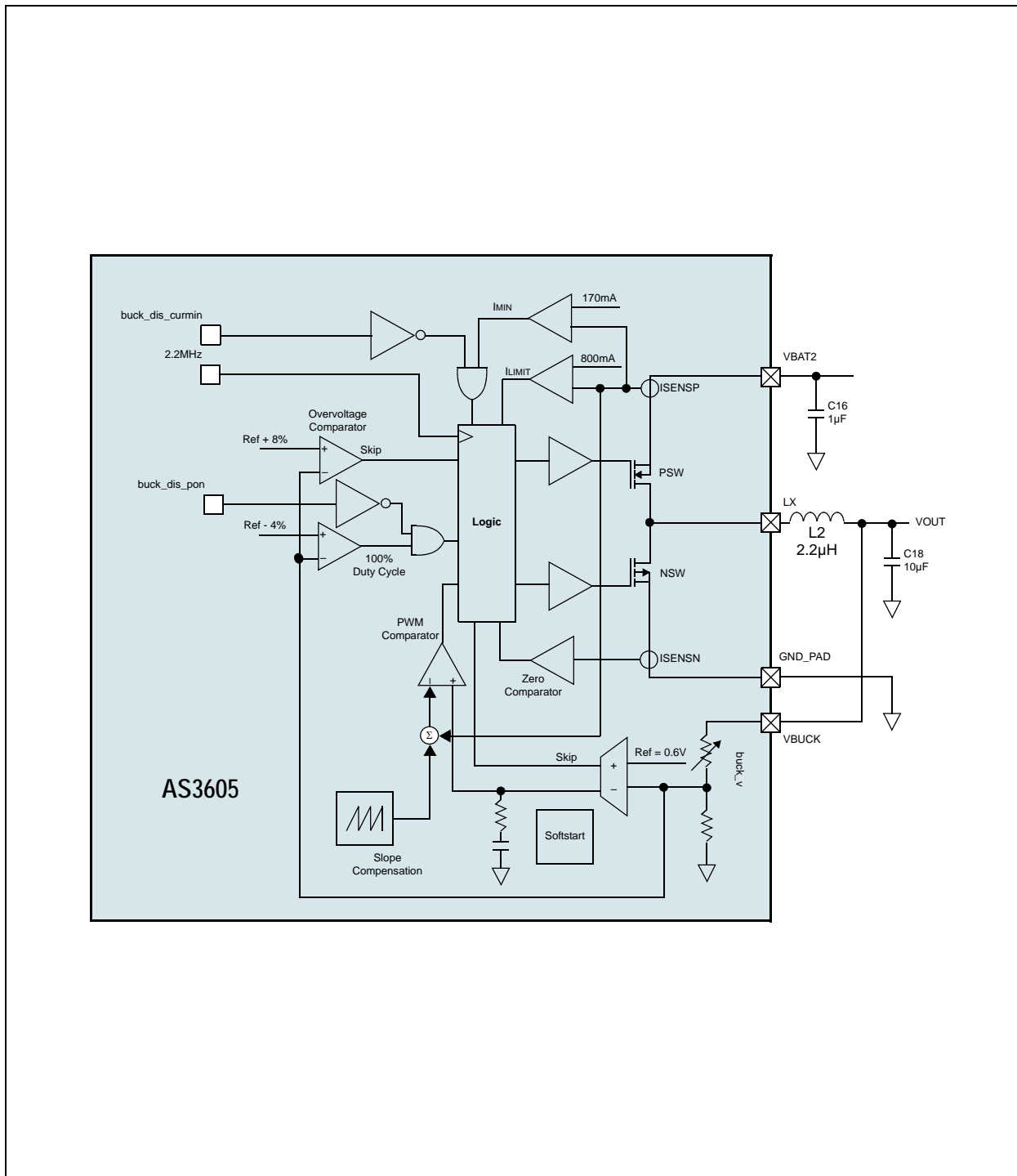
Table 7. Step Down DC/DC Converter Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{IN}	Input Voltage	3.0		5.5	V	Pin VBAT_2
V_{OUT}	Regulated Output Voltage	0.6		3.4	V	Sense pin VBUCK
V_{OUT_TOL}	Output Voltage Tolerance	-50		50	mV	Sense pin VBUCK; Output Voltage < 1.6V
		-3%		3%		Sense pin VBUCK; Output Voltage > 1.6V
I_{LIMIT}	Current Limit		900		mA	Supply current into PMOS transistor
R_{PSW}	PSW On-Resistance			0.5	Ω	
R_{NSW}	NSW On-Resistance			0.5	Ω	
I_{LOAD}	Load Current	0		500	mA	
f_{SW}	Switching Frequency		2.2		MHz	
C_{OUT}	Output Capacitor		10		µF	Ceramic
L_x	Inductor		2.2		µH	
h	Efficiency		90		%	I_{LOAD} = 100mA, V_{OUT} = 2.3V, V_{BAT} = 3V
I_{VDD_DCDC}	Current Consumption		250		µA	Operating Current; No Load
			100			Quiescent Current; Low-Power Mode
			0.1			Shutdown Current
t_{MIN_ON}	Minimum ON Time		80		ns	
t_{MIN_OFF}	Minimum OFF Time		40		ns	

To allow optimized performance in different applications, there are bit settings possible, to get the best compromise between high efficiency and low input/output ripple.

7.2.1 Low-Ripple, Low-Noise Operation

Low-ripple, low-noise operation can be enabled by setting bit **buck_dis_curmin** = 1. In this mode there is no minimum coil current necessary before switching OFF the PMOS. As result, the ON time of the PMOS will be reduced down to t_{MIN_ON} at no or light load conditions, even if the coil current is very small or the coil current is inverted. This results in a very low ripple and noise (but decreased efficiency) at light loads, especially at low input-to-output voltage differences.

Note: Because of the inverted coil current in that case the regulator will not operate in pulse skip mode.

Figure 6. Bit buck_dis_curmin = 1 Operation
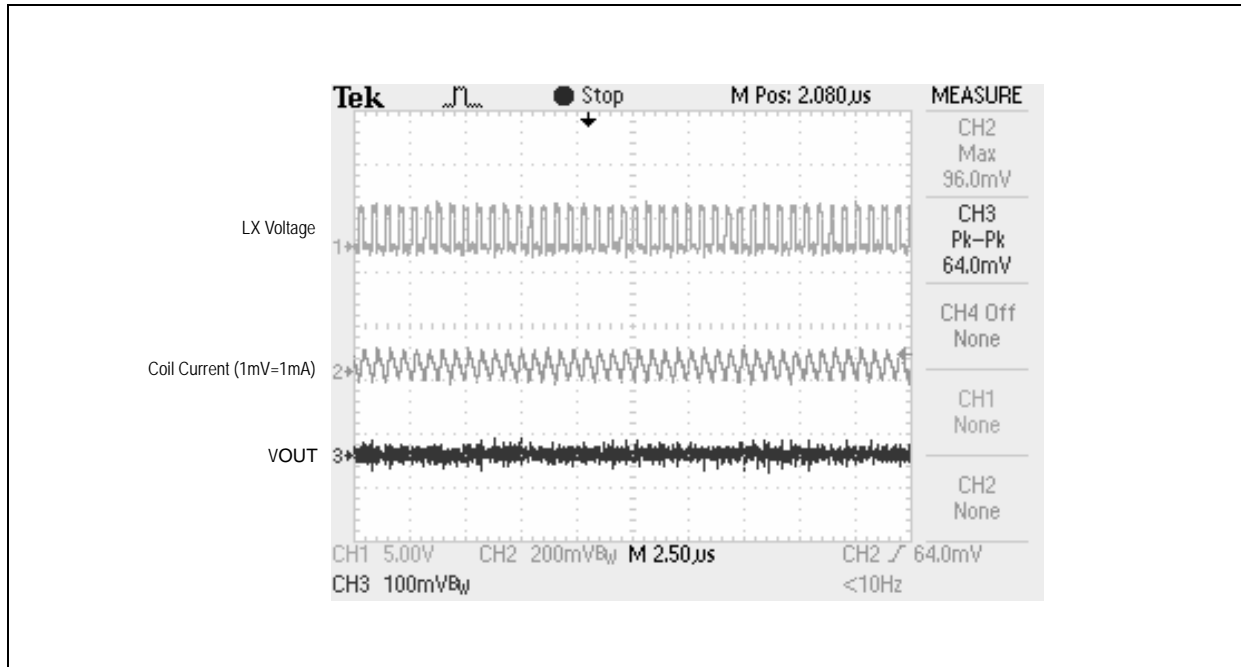
7.2.2   High-Efficiency Operation (Default Setting)

High-efficiency operation is enabled by setting bit **buck_dis_curmin** = 0. In this mode there is a minimum coil current necessary before switching OFF the PMOS. As result there are less pulses at low output load necessary, and therefore the efficiency at low output load is increased. This results in higher ripple, and noisy pulse skip operation up to a higher output current.

Figure 7. Bit buck_dis_curmin = 0 Operation
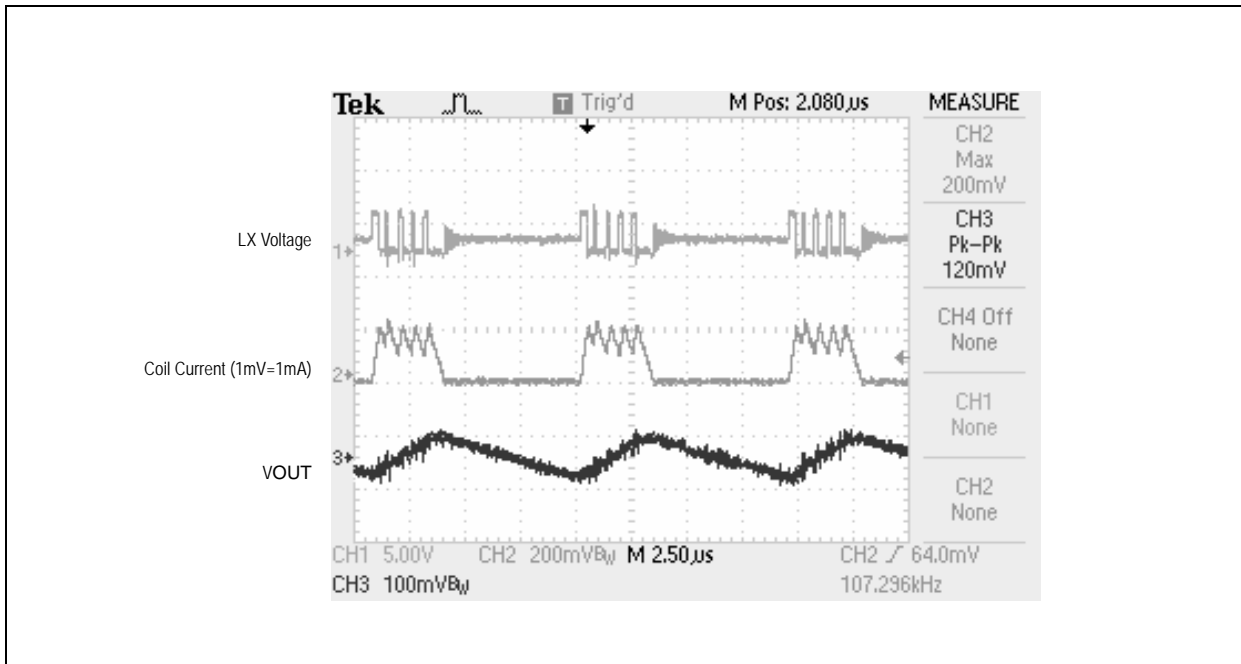
Note: It is possible to switch between these two modes during operation, i.e.:

Bit **buck_dis_curmin** = 0: System is in idle state. No audio or RF signal. Decreased supply current preferred. Increase ripple doesn't effect system performance.

Bit **buck_dis_curmin** = 1: System is operating. Audio signal on and/or RF signal used. Decreased ripple and noise preferred. Increased power supply current can be tolerated.

7.2.3   100% PMOS ON Mode for Low Dropout Regulation

For low input-to-output voltage difference bit **buck_dis_pon** can be set to allow 100% duty cycle of the PMOS transistor, if the output voltage drops by more than 4% below regulation.

7.2.4   Low Power Mode

Bit **buck_lpo** can be set all the time. This mode allows internal power down, of not used blocks during pulseskip mode, which results in a better efficiency at light output loads.

7.2.5   Typical Performance Characteristics

Figure 8. DC/DC Step-Down Efficiency vs. Output Current (buck_dis_cfm = 0)
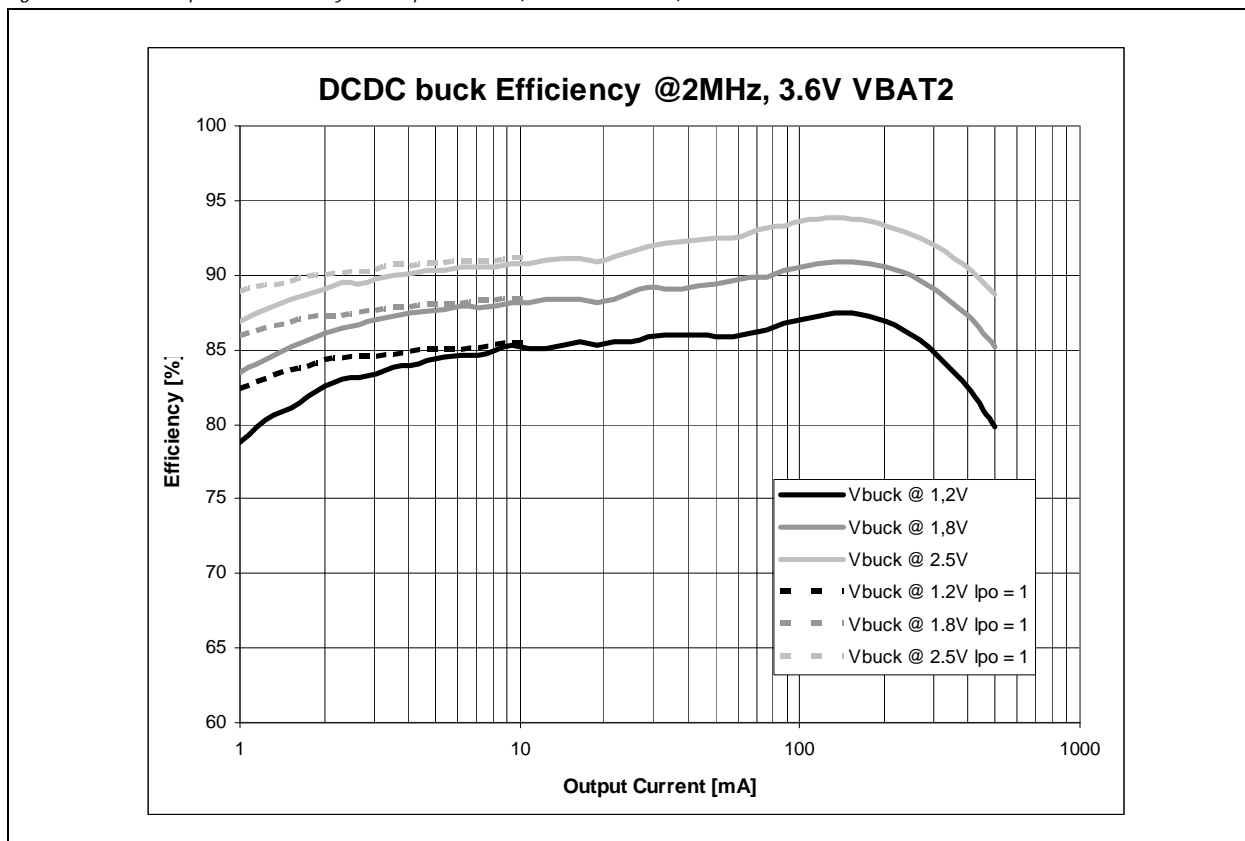
7.2.6   Step Down DC/DC Converter Registers

The Step Down DC/DC Converter is controlled by the registers listed in Table 8.

Table 8. Step Down DC/DC Converter Register Summary

Name	Addr.	b7	b6	b5	b4	b3	b2	b1	b0	Page
Step Down Voltage/Test Modes	01h	-		buck_v						20
Reg Power	09h	-		buck_on	ldo_sim_on			ldo_ana2_on	ldo_ana1_on	20
Step Down Configuration	17h	buck_dis_curmin	buck_dis_pon	buck_lpo	-	-	buck_dis_n	buck_nsw_on	buck_psw_on	20

Step Down Voltage Register (Address 01h).

Addr: 01h				Step Down Voltage/Test Modes	
				Sets the output voltage of the Step Down DC/DC Converter.	
Bit	Bit Name	Default	Access	Bit Description	
5:0	buck_v	Boot ROM	R/W	Controls the voltage selection for the Step Down DC/DC Converter.	
				000000	0.6V
				…	(LSB = 50mV)
				111000-111111	3.4V
7:6	-	NA	NA		

Reg Power Register (Address 09h).

Addr: 09h				Reg Power	
				Enables/disables voltage regulators.	
Bit	Bit Name	Default	Access	Bit Description	
0	ldo_ana1_on	Boot ROM	RW	Refer to page 28	
1	ldo_ana2_on	Boot ROM	RW	Refer to page 28	
3:2	-	NA	NA		
4	ldo_sim_on	Boot ROM	RW	Refer to page 28	
5	buck_on	Boot ROM	R/W	Enables the Step Down DC/DC Converter.	
				0	Step Down DC/DC Converter is OFF.
				1	Step Down DC/DC Converter is ON.
7:6	-	NA	NA		

Step Down Configuration Register (Address 17h).

Addr: 17h				Step Down Configuration	
				Configures the operation mode of the Step Down DC/DC Converter.	
Bit	Bit Name	Default	Access	Bit Description	
0	buck_psw_on	0	R/W	Activate PSW (0.5Ω PMOS) only if **buck_on** and **buck_nsw_on** = 0.	
				0	Default setting. P-Channel switching transistor is controlled by the DC/DC Converter.
				1	Turns on P-Channel switching transistor. Bits **buck_on** and **buck_nsw_on** must both = 0.
1	buck_nsw_on	0	R/W	Activates NSW (0.5Ω NMOS) only if **buck_on** = 0 and **buck_psw_on** = 0.	
				0	Default setting. N-Channel switching transistor is controlled by the DC/DC Converter.
				1	Turns on N-Channel switching transistor. Bits **buck_on** and **buck_psw_on** must both = 0.
2	buck_dis_n	0	R/W	0	Default setting. Normal operation of The synchronous rectifier.
				1	The synchronous rectifier is disabled (NSW is always OFF).
3	-	0	RW	0	
				1	

Addr: 17h				Step Down Configuration	
				Configures the operation mode of the Step Down DC/DC Converter.	
Bit	Bit Name	Default	Access	Bit Description	
4	-	0	R/W		
				0	
				1	
5	buck_lpo	0	R/W	0	Low-power mode disabled.
				1	Low-power mode enabled.
6	buck_dis_pon	0	R/W	Step down PON feature control.	
				0	PON feature enabled. 100% duty cycle (PMOS always on) if output voltage drops more than 4%. Increased output ripple in that operation.
				1	PON feature disabled. Maximum duty cycle = 1 - (tmin_off*fsw)
7	buck_dis_curmin	0	R/W	Step down current force mode	
				0	current force mode enabled. Inductor current regulated to min 170mA. Higher efficiency in low dropout and low output current operation. Higher output ripple and noise.
				1	current force mode disabled. Decreased efficiency in low dropout mode and at low output current. Small output ripple and noise.

7.3 Low Dropout Regulators

The Low Dropout Regulators (LDOs) are linear high performance regulators with programmable output voltages. The LDOs can be controlled by either software (voltage, ON/OFF) or hardware (ON/OFF) using highly configurable GPIO1 to GPIO3 pins.

The Low Dropout Regulators include the following:

■ RF and Analog Low Dropout Regulators – Described on page 22

■ Analog LDO Block Diagram – Described on page 22

■ SIMCard Low Dropout Regulator – Described on page 23

■ Low Power Low Dropout Regulator – Described on page 24

7.3.1 RF and Analog Low Dropout Regulators

The RF LDOs (VRF_1 - VRF_4) and Analog LDOs (VANA_1 and VANA_2) are designed to supply power to sensitive analog circuits like LNAs, Transceivers, VCOs and other critical RF components of cellular radios. Additionally, these LDOs are suitable for supplying power to audio devices or as a reference for A/D and D/A converters.

The design is optimized to deliver the best compromise between quiescent current and regulator performance for battery powered devices. Stability is guaranteed with ceramic output capacitors (see Figure) of 1μF ±20% (X5R) or 2.2μF +100 / -50% (Z5U).

The low ESR of these capacitors ensures low output impedance at high frequencies. Regulation performance is excellent even under low dropout conditions, when the power transistor has to operate in linear mode. Power supply rejection is high enough to suppress ripple on the battery caused by the PA in TDMA systems. The low noise performance allows direct connection of noise sensitive circuits without additional filtering networks. The low impedance of the power transistor enables the device to deliver up to 150mA even at nearly discharged batteries without any decrease of performance.

The LDOs have a built-in discharge function when switched off.

Figure 9. Analog LDO Block Diagram
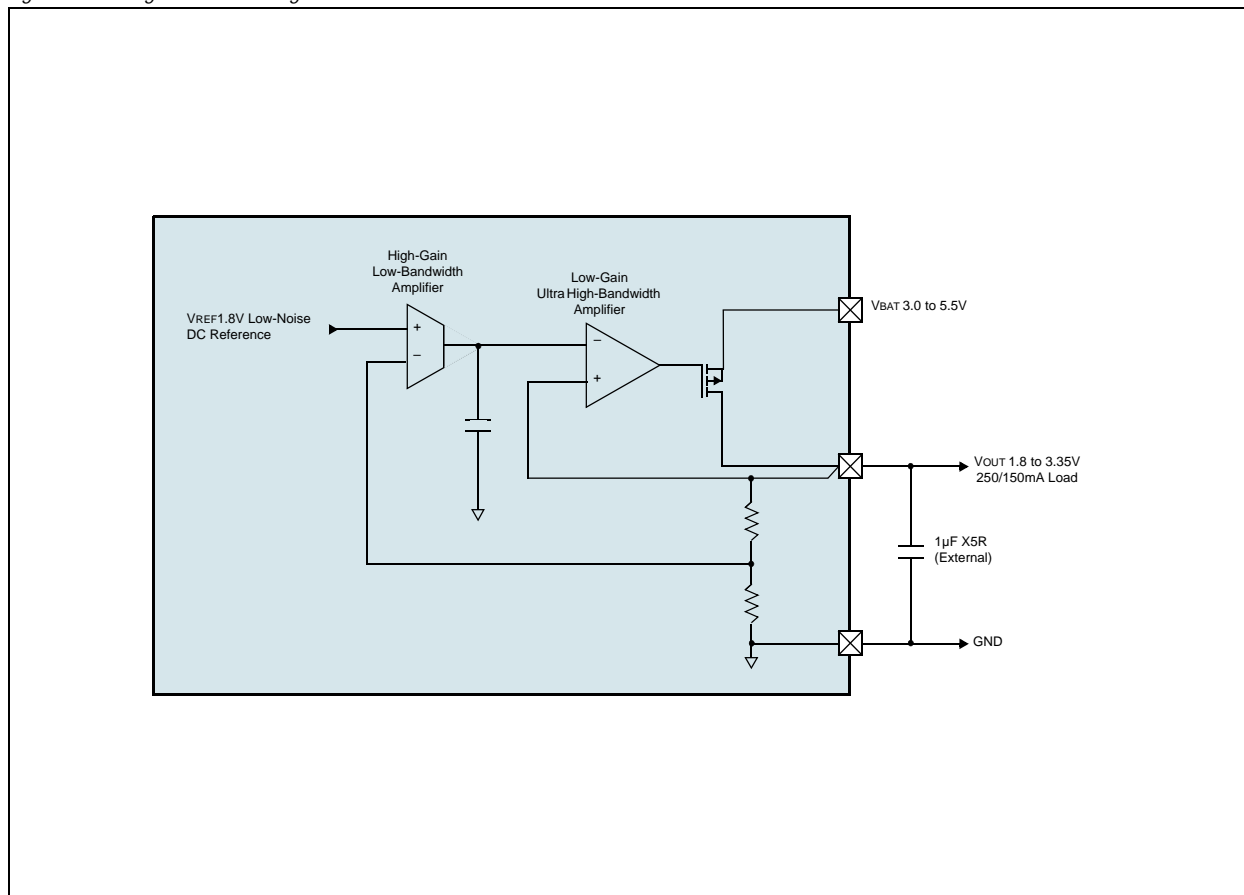
Table 9. RF and Analog LDO Characteristics
V_{BAT} = 3.6V; I_{LOAD} = 150mA; T_A = 25ºC; C_{LOAD} = 2.2µF (Ceramic); unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{BAT}	Supply Voltage Range	3		5.5	V	
R_{ON}	On-Resistance			1	Ω	VANA_1, VANA_2
				2		VRF_1, VRF_2, VRF_3, VRF_4
PSRR	Power Supply Rejection Ratio	70			dB	f = 1kHz
		40				f = 100kHz
I_{OFF}	Shut Down Current			100	nA	
I_{VDD_LDO}	Supply Current			50	µA	Without load
Noise	Output Noise		30	50	µVrms	10Hz < f < 100kHz
t_{START}	Startup Time			200	µs	
V_{OUT}	Output Voltage	1.8		2.85	V	V_{BAT} > 3.0V
		1.8		3.35		Full programmable range
V_{OUT_TOL}	Output Voltage Tolerance	-50		50	mV	
$V_{LINEREG}$	Line Regulation	-1		1	mV	Static
		-10		10		Transient; Slope: t_r = 10µs
$V_{LOADREG}$	Load Regulation	-1		1	mV	Static
		-10		10		Transient; Slope: t_r = 10µs
I_{LIMIT}	Current Limitation	250	400		mA	VANA_1, VANA_2
		150	180		mA	VRF_1, VRF_2, VRF_3, VRF_4

7.3.2   SIMCard Low Dropout Regulator

The SIMCard LDO (VSIM) is optimized for SIMCard supply. It is designed to achieve the lowest possible power consumption and still provide reasonable regulation characteristics. To ensure high PSRR and stability, a low-ESR ceramic capacitor of 100nF (min.) must be connected to the output. The LDO has a built-in discharge function when switched off.

Table 10. LDO VSIM Characteristics
V_{BAT} = 3.6V; I_{LOAD} = 20mA; T_A = 25ºC; C_{LOAD} = 100nF (Ceramic); unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{BAT}	Supply Voltage Range	3		5.5	V	
R_{ON}	On-Resistance			50	Ω	
PSRR	Power Supply Rejection Ratio	40			dB	f = 1kHz
		20				f = 100kHz
I_{OFF}	Shut Down Current			100	nA	
$I_{VDD\_SIMCARD}$	Supply Current		40		µA	
t_{START}	Startup Time			200	µs	
V_{OUT}	Output Voltage	1.8		3.0	V	V_{BAT} > 3.2V
V_{OUT_TOL}	Output Voltage Tolerance	-50		50	mV	
$V_{LINEREG}$	Line Regulation	-10		10	mV	Static
		-100		100		Transient; Slope: t_r = 10µs

Table 10. LDO VSIM Characteristics (Continued)
V_{BAT} = 3.6V; I_{LOAD} = 20mA; T_A = 25ºC; C_{LOAD} = 100nF (Ceramic); unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{LOADREG}$	Load Regulation	-10		10	mV	Static
		-100		100		Transient; Slope: t_r = 10µs

7.3.3 Low Power Low Dropout Regulator

The low-power bootstrap LDO (V2_5) is needed to supply power to the core (analog and digital) of the AS3605. LDO V2_5 is designed to achieve the lowest possible power consumption, and still provide reasonable regulation characteristics. LDO V2_5 has two supply inputs selecting automatically the higher one. This gives the possibility to supply the AS3605 core either with the battery or with the Battery Charger, depending on the conditions.

To ensure high PSRR and stability, a low-ESR ceramic capacitor of 1µF (min.) must be connected to the output.

Note: Levelshifters in both directions (input and output) are placed between digital pins (VANA_1) and the digital core (V2_5) of the device, because of the different power supplies.

Table 11. LDO V2_5 Characteristics
V_{BAT} = 3.6V; C_{LOAD_EXT} = 0; T_A = 25ºC; C_{LOAD} = 2.2µF (Ceramic); unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{BAT}	Supply Voltage Range	2.8		5.5	V	
$V_{CHARGER}$	External Charger Adapter voltage	4		15	V	
R_{ON}	On-Resistance		50		Ω	Guaranteed per design
I_{OFF}	Shut Down Current			100	nA	
I_{VDD_LPLDO}	Supply Current			3	µA	Guaranteed per design; consider device internal load for measurement
t_{START}	Startup Time			200	µs	
V_{OUT}	Output Voltage	2.4	2.5	2.6	V	

7.3.4   Typical Performance Characteristics

Figure 10. Load Regulation of LDOs VANA_1, VANA_2
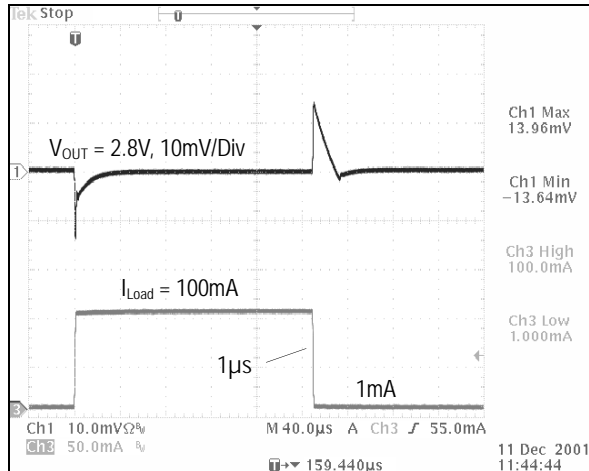
X-Axis: 40µs/Div

Figure 11. Output Noise of LDOs VANA_1, VANA_2
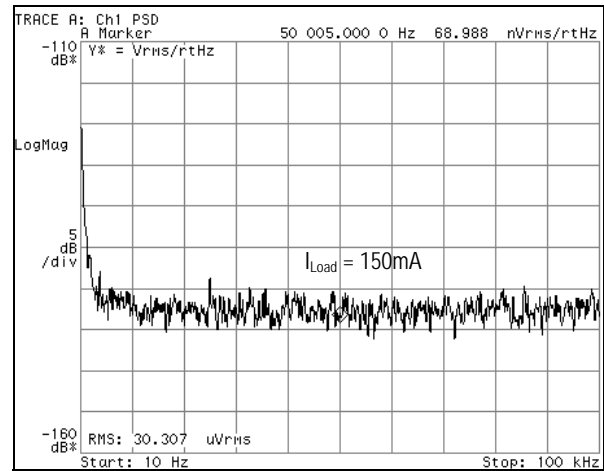
Spectral Distribution at 150mA Output Load

Figure 12. Load Regulation of LDO V2_5
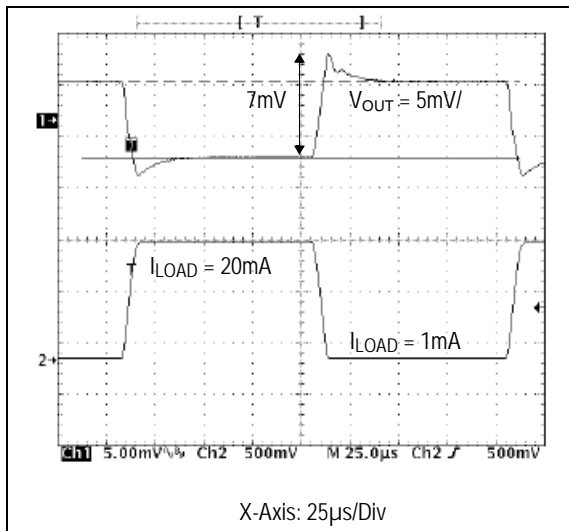
X-Axis: 25µs/Div

Figure 13. Line Regulation of LDO V2_5
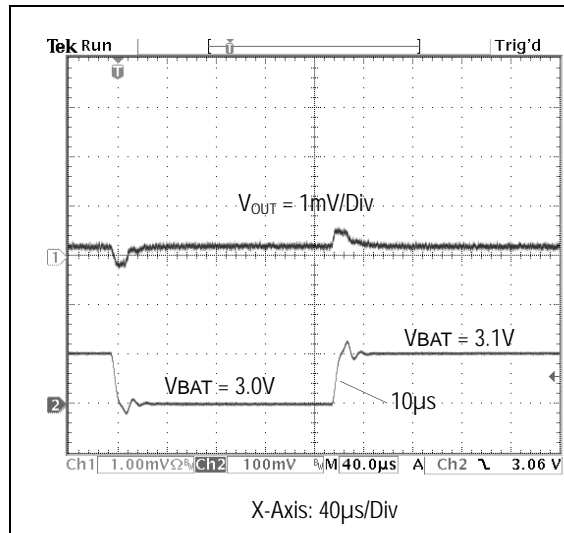
X-Axis: 40µs/Div

7.3.5   LDO Registers

The Low Dropout Regulators are controlled by the registers listed in Table 12.

Table 12. Low Dropout Regulators Register Summary

Name	Addr.	b7	b6	b5	b4	b3	b2	b1	b0	Page
LDO_RF1 Voltage	02h	-			ldo_rf1_v					26
LDO_RF2 Voltage	03h	-			ldo_rf2_v					27
LDO_RF3 Voltage	04h	-			ldo_rf3_v					27
LDO_RF4 Voltage	05h	-			ldo_rf4_v					27
LDO_ANA2_Voltage	06h	-			ldo_ana2_v					27
LDO_ANA1_Voltage	07h	-			ldo_ana1_v					28
LDO_SIM_Voltage	08h	-	ldo_sim_v	-						28
Reg Power	09h	-		buck_on	ldo_sim_on	-	-	ldo_ana2_on	ldo_ana1_on	28
LDO_GPIO Active	0Fh	-	-	ldo_rf4_gpio	ldo_rf3_gpio	ldo_rf2_gpio	ldo_rf1_gpio	ldo_ana2_gpio	ldo_buck_gpio	29
LDO_CHG	10h	ldo_rf4_on	ldo_rf3_on	ldo_rf2_on	ldo_rf1_on	EOCCurrent[1:0]		ana2_sw	ana1_sw	29
LDO_AD GPIOx	11h	-				ldo_ana2_gpio_sel		buck_gpio_sel		30
LDO_RF GPIOx	12h	ldo_rf4_gpio_sel		ldo_rf3_gpio_sel		ldo_rf2_gpio_sel		ldo_rf1_gpio_sel		31

LDO_RF1 Voltage Register (Address 02h).

Addr: 02h		LDO_RF1 Voltage				
		Sets the voltage for LDO VRF_1.				
Bit	Bit Name	Default	Access	Bit Description		
4:0	ldo_rf1_v	Boot ROM	R/W	00000	1.8V	
				…	(LSB = 50mV)	
				11111	3.35V	
7:5	-	NA	NA			

LDO_RF2 Voltage Register (Address 03h).

Addr: 03h		LDO_RF2 Voltage			
		Sets the voltage for LDO VRF_2.			
Bit	Bit Name	Default	Access	Bit Description	
4:0	ldo_rf2_v	Boot ROM	R/W	00000	1.8V
				…	(LSB = 50mV)
				11111	3.35V
7:5	-	NA	NA		

LDO_RF3 Voltage Register (Address 04h).

Addr: 04h		LDO_RF3 Voltage			
		Sets the voltage for LDO VRF_3.			
Bit	Bit Name	Default	Access	Bit Description	
4:0	ldo_rf3_v	Boot ROM	R/W	00000	1.8V
				…	(LSB = 50mV)
				11111	3.35V
7:5	-	NA	NA		

LDO_RF4 Voltage Register (Address 05h).

Addr: 05h		LDO_RF4 Voltage			
		Sets the voltage for LDO VRF_4.			
Bit	Bit Name	Default	Access	Bit Description	
4:0	ldo_rf4_v	Boot ROM	R/W	00000	1.8V
				…	(LSB = 50mV)
				11111	3.35V
7:5	-	NA	NA		

LDO_ANA2_Voltage Register (Address 06h).

Addr: 06h		LDO_ANA2_Voltage			
		Sets the voltage for LDO VANA_2.			
Bit	Bit Name	Default	Access	Bit Description	
4:0	ldo_ana2_v	Boot ROM	R/W	Sets the voltage for LDO VANA_2	
				00000	1.80V
				…	(LSB = 50mV)
				11111	3.35V
7:5	-	NA	NA		

LDO_ANA1_Voltage Register (Address 07h).

Addr: 07h				LDO_ANA1_Voltage	
				Sets the voltage for LDO VANA_1.	
Bit	Bit Name	Default	Access	Bit Description	
4:0	ldo_ana1_v	Boot ROM	R/W	Sets the voltage for LDO VANA_1	
				00000	1.8V
				...	(LSB = 50mV)
				11111	3.35V
7:5	-	NA	NA		

LDO_SIM_Voltage Register (Address 08h).

Addr: 08h				LDO_SIM_Voltage	
				Sets the voltage for Digital LDO VSIM.	
Bit	Bit Name	Default	Access	Bit Description	
5:0	-	NA	NA		
6	ldo_sim_v	Boot ROM	R/W	Sets the voltage for LDO VSIM.	
				0	1.8V
				1	3.0V
7	-	NA	NA		

Reg Power Register (Address 09h).

Addr:09h				Reg Power	
				Enables/disables voltage regulators.	
Bit	Bit Name	Default	Access	Bit Description	
0	ldo_ana1_on	Boot ROM	R/W	Enables control of LDO VANA_1. **Note:** Do not set this bit = 0 or serial interface access will be disabled.	
				0	LDO VANA_1 is OFF.
				1	LDO VANA_1 is ON.
1	ldo_ana2_on	Boot ROM	R/W	Enables control of LDO VANA_2.	
				0	LDO VANA_2 is OFF.
				1	LDO VANA_2 is ON.
3:2	-	NA	NA		
4	ldo_sim_on	Boot ROM	R/W	Enables control of LDO VSIM.	
				0	LDO VSIM is OFF.
				1	LDO VSIM is ON.
5	buck_on	Boot ROM		Enables the Step Down DC/DC Converter.	
				0	Step Down DC/DC Converter is OFF.
				1	Step Down DC/DC Converter is ON.
7:6	-	NA	NA		

LDO_GPIO Active Register (Address 0Fh).

Addr: 0Fh		LDO_GPIO Active			
		Activates GPIO ON/OFF control for voltage regulators.			
Bit	Bit Name	Default	Access	Bit Description	
0	buck_gpio	Boot ROM	R/W	Activates GPIO control of Step Down DC/DC Converter.	
				0	Controlled by software.
				1	On when assigned GPIO pin = 1 and bit **buck_on** = 1.
1	ldo_ana2_gpio	Boot ROM	R/W	Activates GPIO control for LDO VANA_2.	
				0	Controlled by software.
				1	On when assigned GPIO pin = 1 and bit **ldo_ana2_on** = 1.
2	ldo_rf1_gpio	Boot ROM	R/W	Activates GPIO control for LDO VRF_1.	
				0	Controlled by software.
				1	On when assigned GPIO pin = 1 and bit **ldo_rf1_on** = 1.
3	ldo_rf2_gpio	Boot ROM	R/W	Activates GPIO control for LDO VRF_2.	
				0	Controlled by software.
				1	On when assigned GPIO pin = 1 and bit **ldo_rf2_on** = 1.
4	ldo_rf3_gpio	Boot ROM	R/W	Activates GPIO control for LDO VRF_3.	
				0	Controlled by software.
				1	On when assigned GPIO pin = 1 and bit **ldo_rf3_on** = 1.
5	ldo_rf4_gpio	Boot ROM	R/W	Activates GPIO control for LDO VRF_4.	
				0	Controlled by software.
				1	LDO VRF_4 is on when assigned GPIO pin = 1 and bit **ldo_rf4_on** = 1.
7:6	-	NA	NA		

LDO_RF Switch Register (Address 10h).

Addr: 10h		LDO_CHG			
		Enables LDOs and high-side switches.			
Bit	Bit Name	Default	Access	Bit Description	
0	ana1_sw	0	R/W	0	VANA_1 operates as LDO.
				1	VANA_1 is operating as high-side switch ($R_{ON}=1\Omega$); valid if **ldo_ana1_on** = 0.
1	ana2_sw	0	R/W	0	VANA_2 operates as LDO.
				1	VANA_2 is operating as high-side switch ($R_{ON}=1\Omega$); valid if **ldo_ana2_on** = 0.
4	ldo_rf1_on	0	R/W	Enables control of LDO VRF_1.	
				0	LDO VRF_1 is OFF.
				1	LDO VRF_1 is ON.

Addr: 10h		LDO_CHG				
		Enables LDOs and high-side switches.				
Bit	Bit Name	Default	Access	Bit Description		
5	ldo_rf2_on	0	R/W	Enables control of LDO VRF_2.		
				0	LDO VRF_2 is OFF.	
				1	LDO VRF_2 is ON.	
6	ldo_rf3_on	0	R/W	Enables control of LDO VRF_3.		
				0	LDO VRF_3 is OFF.	
				1	LDO VRF_3 is ON.	
7	ldo_rf4_on	0	R/W	Enables control of LDO VRF_4.		
				0	LDO VRF_4 is OFF.	
				1	LDO VRF_4 is ON.	

ldo_anax_on*	anax_sw*	ANA LDO Function
0	0	OFF
0	1	Fully ON, R_{ON} = 1Ω
1	0	Linear Voltage Regulator
1	1	Not Allowed

* Where x = 1-4

LDO_AD GPIOx Register (Address 11h).

Addr: 11h		LDO_AD GPIOx				
		Selects GPIO pin for power ON/OFF control for DCDC and VANA_2.				
Bit	Bit Name	Default	Access	Bit Description		
1:0	buck_gpio_sel	00$_h$	R/W	Valid if GPIO activation bit **buck_gpio** = 1		
				00	GPIO1	
				01	GPIO2	
				10	GPIO3	
				11	Do not use this setting	
3:2	ldo_ana2_gpio_sel	00$_h$	R/W	Valid if GPIO activation bit **ldo_ana2_gpio** = 1		
				00	GPIO1	
				01	GPIO2	
				10	GPIO3	
				11	Do not use this setting	
7:4	NA					

LDO_RF GPIOx Register (Address 12h).

Addr: 12h		LDO_RF GPIOx			
		Selects GPIO pin for power ON/OFF control for RF LDOs VRF_1 - VRF_4.			
Bit	Bit Name	Default	Access	Bit Description	
1:0	ldo_rf1_gpio_sel	Boot ROM	R/W	Valid if **ldo_rf1_gpio** = 1	
				00	GPIO1
				01	GPIO2
				10	GPIO3
				11	Do not use this setting
3:2	ldo_rf2_gpio_sel	Boot ROM	R/W	Valid if **ldo_rf2_gpio** = 1	
				00	GPIO1
				01	GPIO2
				10	GPIO3
				11	Do not use this setting
5:4	ldo_rf3_gpio_sel	Boot ROM	R/W	Valid if **ldo_rf3_gpio** = 1	
				00	GPIO1
				01	GPIO2
				10	GPIO3
				11	Do not use this setting
7:6	ldo_rf4_gpio_sel	Boot ROM	R/W	Valid if **ldo_rf4_gpio** = 1	
				00	GPIO1
				01	GPIO2
				10	GPIO3
				11	Do not use this setting

7.4 Charge Pump

The Charge Pump uses the external flying capacitor C2 (470nF) to generate output voltages higher than the battery voltage. There are two different operating modes of the charge pump itself:

■ 1:1 Bypass Mode

  - Battery input and output are connected by a low-impedance switch
  - Battery current = output current

■ 1:2 Mode

  - The output voltage is up to 2 times the battery voltage (without load), but is limited to VCPOUTmax all the time
  - Battery current = 2 times output current

As the battery voltage decreases, the Charge Pump must be switched from 1:1 mode to 1:2 mode in order to provide enough supply for the current sinks. Depending on the actual current, the mode with best overall efficiency can be automatically or manually selected:

The charge pump mode switching can be done manually or automatically with the following possible software settings:

■ Automatic

  - Start with 1:1 mode
  - Switch up automatically to 1:2 mode

■ Manual

  - Set modes 1:1 and 1:2 by software

7.4.1 Charge Pump Mode Switching

If automatic mode switching is enabled (**cp_mode_switching** = 0) the charge pump monitors the current sinks, which are connected via a LED to the output V5_6. To identify these current sources (sinks), the registers CP mode Switch (register bits **curr1_on_cp** ...**curr5_on_cp**) should be setup before starting the charge pump (**cp_on** =1). If any of the voltage on these current sources drops below the threshold (currlv_switch, currhv_switch), the 1:2 mode is selected after the debounce time. The CP will not switch back to 1:1 mode.

If the currX_on_cp=0 and the according current sink is connected to the charge pump, the current sink will be functional, but there is no up switching of the charge pump, if the voltage compliance is too low for the current sink to supply the specified current.

Figure 14. Automatic Mode Switching
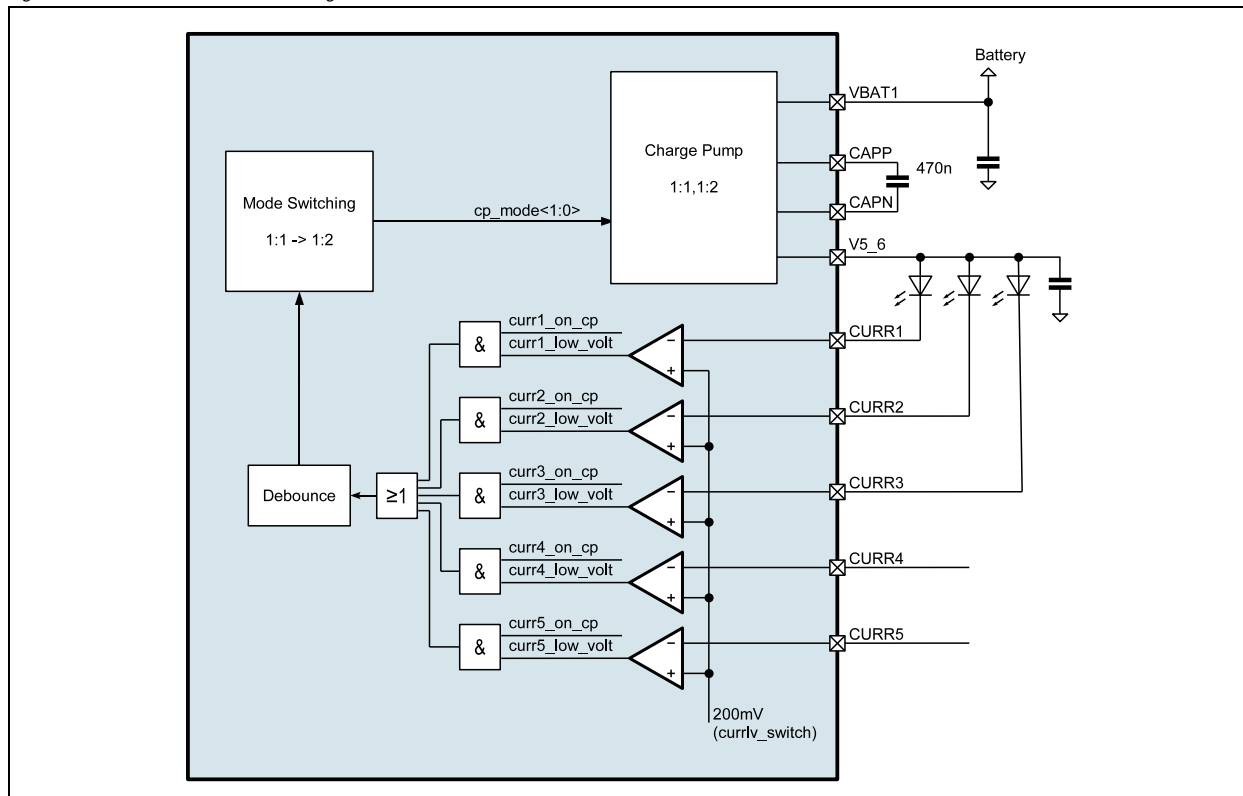
The Charge Pump requires the external components specified in Table 13.

Table 13. Charge Pump External Components

Symbol	Parameter	Min	Typ	Max	Unit	Notes
C$_{FLY}$ (C2)	External Flying Capacitor		470		nF	Ceramic low-ESR capacitor between pins CAPP and CAPN (see page 2).
C$_{STORE}$ (C3)	External Storage Capacitor	1		4.7	µF	Ceramic low-ESR capacitor between pins V5_6 and VSS (see page 2).

Note: Connections to the two external capacitors should be kept as short as possible.

Table 14. Charge Pump Parameters
V$_{BAT}$ = 3.6V; T$_{AMB}$ = 25ºC; unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I$_{CPOUT}$	Output Current	0		60	mA	
V$_{CPOUTmax}$	Output Voltage			5.6	V	including output ripple
R$_{CP}$	Effective Charge Pump Output Resistance		8.8		Ω	V$_{BAT}$ = 3.0V, **cp_mode[1:0]** = 1:1
			31		Ω	V$_{BAT}$ = 3.0V, **cp_mode[1:0]** = 1:2
currlv_switch	if the current sink voltage drops below this threshold it will change from 1:1 to 1:2 mode			200	mV	**cp_mode_switching** = automatic
t$_{deb}$	start_up debounce time		240		µs	**cp_start_debounce** = 0
			2000			**cp_start_debounce** = 1
I$_{SHUTDOWN}$	Shutdown Current			0.1	µA	

7.4.2   Charge Pump Registers

Table 15. Charge Pump Register Summary

Name	Addr.	b7	b6	b5	b4	b3	b2	b1	b0	Page
Charge Pump Control Onkey Pulldown	18h	cp_auto_on	cp_start_debounce	onkey_pulld_off	cp_freq	cp_mode_switching	cp_mode[1:0]		cp_on	34
CP Mode Switch	36h	NA			curr5_on_cp	curr4_on_cp	curr3_on_cp	curr2_on_cp	curr1_on_cp	35
Curr Low Voltage Status	37h	NA			curr5_low_volt	curr4_low_volt	curr3_low_volt	curr2_low_volt	curr1_low_volt	35

Charge Pump Control Onkey Pulldown Register (Address 18h).

Addr: 18h		Charge Pump Control Onkey Pulldown			
		Sets the operation mode of the Charge Pump.			
Bit	Bit Name	Default	Access	Bit Description	
0	cp_on	0b	R/W	0	Set CP into 1:1 mode (OFF state) unless **cp_auto_on** is set.
				1	Enable manual mode switching
2:1	cp_mode[1:0]	00b	R/W	CP mode (in manual mode sets this mode, in automatic mode reports the actual mode used)	
				00	1:1 mode
				01	
				10	1:2 mode
				11	
3	cp_mode_switching	0b	R/W	Set the mode switching algorithm	
				0	Automatic mode switching
				1	Manual mode switching; register **cp_mode[1:0]** defines the actual CP mode used.
4	cp_freq	0b	R/W	Clock frequency selection	
				0	1 MHz
				1	500 kHz
5	onkey_pulld_off	0b	R/W	0	pull down on ON-key active
				1	pull down on ON-key deactivated
6	cp_start_debounce	0b	R/W	0	Mode switching debounce timer is always 240μs.
				1	Upon startup (**cp_on** set to 1) the mode switching debounce time is first started with 2ms then reduced to 240μs.
7	cp_auto_on	1b	R/W	0	The CP is swiched ON/OFF with **cp_on**
				1	The CP is automatically switched on if a current sink, which is connected to the CP (defined by registers CP Mode Switch 1&2) is switched ON and detects a low voltage condition.

CP Mode Switch Register (Address 36h).

Addr: 36h		CP Mode Switch			
		Setup which current sinks are connected (via LEDs) to the CP; if set to 1 the corresponding current sink is used for automatic mode selection of the CP.			
Bit	Bit Name	Default	Access	Bit Description	
0	curr1_on_cp	0b	R/W	0	Current sink CURR1 is not connected to the CP
				1	Current sink CURR1 is connected to the CP
1	curr2_on_cp	0b	R/W	0	Current sink CURR2 is not connected to the CP
				1	Current sink CURR2 is connected to the CP
2	curr3_on_cp	0b	R/W	0	Current sink CURR3 is not connected to the CP
				1	Current sink CURR3 is connected to the CP
3	curr4_on_cp	0b	R/W	0	Current sink CURR4 is not connected to the CP
				1	Current sink CURR4 is connected to the CP
4	curr5_on_cp	0b	R/W	0	Current sink CURR5 is not connected to the CP
				1	Current sink CURR5 is connected to the CP
5:7	-	NA	NA		

Curr Low Voltage Status Register (Address 37h).

Addr: 37h		Curr Low Voltage Status			
		Indicates the low voltage status of the current sinks. If the currX_low_v bit is set, the voltage on the current sink is too low, to drive the selected output current.			
Bit	Bit Name	Default	Access	Bit Description	
0	curr1_low_v	NA	R	0	The voltage of current sink CURR1 > currlv_switch
				1	The voltage of current sink CURR1 < currlv_switch
1	curr2_low_v	NA	R	0	The voltage of current sink CURR2 > currlv_switch
				1	The voltage of current sink CURR2 < currlv_switch
2	curr3_low_v	NA	R	0	The voltage of current sink CURR3 > currlv_switch
				1	The voltage of current sink CURR3 < currlv_switch
3	curr4_low_v	NA	R	0	The voltage of current sink CURR4 > currlv_switch
				1	The voltage of current sink CURR4 < currlv_switch
4	curr5_low_v	NA	R	0	The voltage of current sink CURR5 > currlv_switch
				1	The voltage of current sink CURR5 < currlv_switch
5:7	-	NA	NA		

7.5 General Purpose Input/Output

The general purpose input/output pins (GPIO1 - GPIO3) are highly configurable and independently controlled.

Table 16. DC Characteristics Input/Output Pin with Selectable Supply GPIO1:GPIO3

Symbol	Parameter	Min	Max	Unit	Notes
V_{IH}	High-Level Input Voltage	0.7 x V_{ANA_1}		V	
V_{IL}	Low-Level Input Voltage		0.3 x V_{ANA_1}	V	
I_{LEAK}	Input Leakage Current (if not used as pulldown/pullup)	-5	5	µA	to VANA_1 and VSS
$I_{PULLDOWN}$	Pulldown Current (if configured as pulldown)	5	50	µA	to VSS
I_{PULLUP}	Pullup Current (if configured as pullup)	-200	-20	µA	to V5_6 or VANA_1 as configured
V_{OH}	High-Level Output Voltage Supply VANA_1	0.8 x V_{ANA_1}		V	at -2mA
V_{OL}	Low-Level Output Voltage		0.2 x V_{ANA_1}	V	at 2mA
C_{LOAD}	Capacitive Load		50	pF	

GPIO1 - GPIO3 can be used to accommodate the following functionality:

- Software controlled input and output
- Input pin for the Watchdog
- Signal input (GPIO1-GPIO3)
- Interrupt output with configurable interrupt source
- Configurable frequency and duty cycle output
- External clock input for Step Up/Down DC/DC Converters and Charge Pump synchronization (GPIO1 only)
- Active pullup or pulldown; can be combined with other I/O functions
- Output open drain (push or pull type)

Figure 15. General Purpose I/O Block Diagram
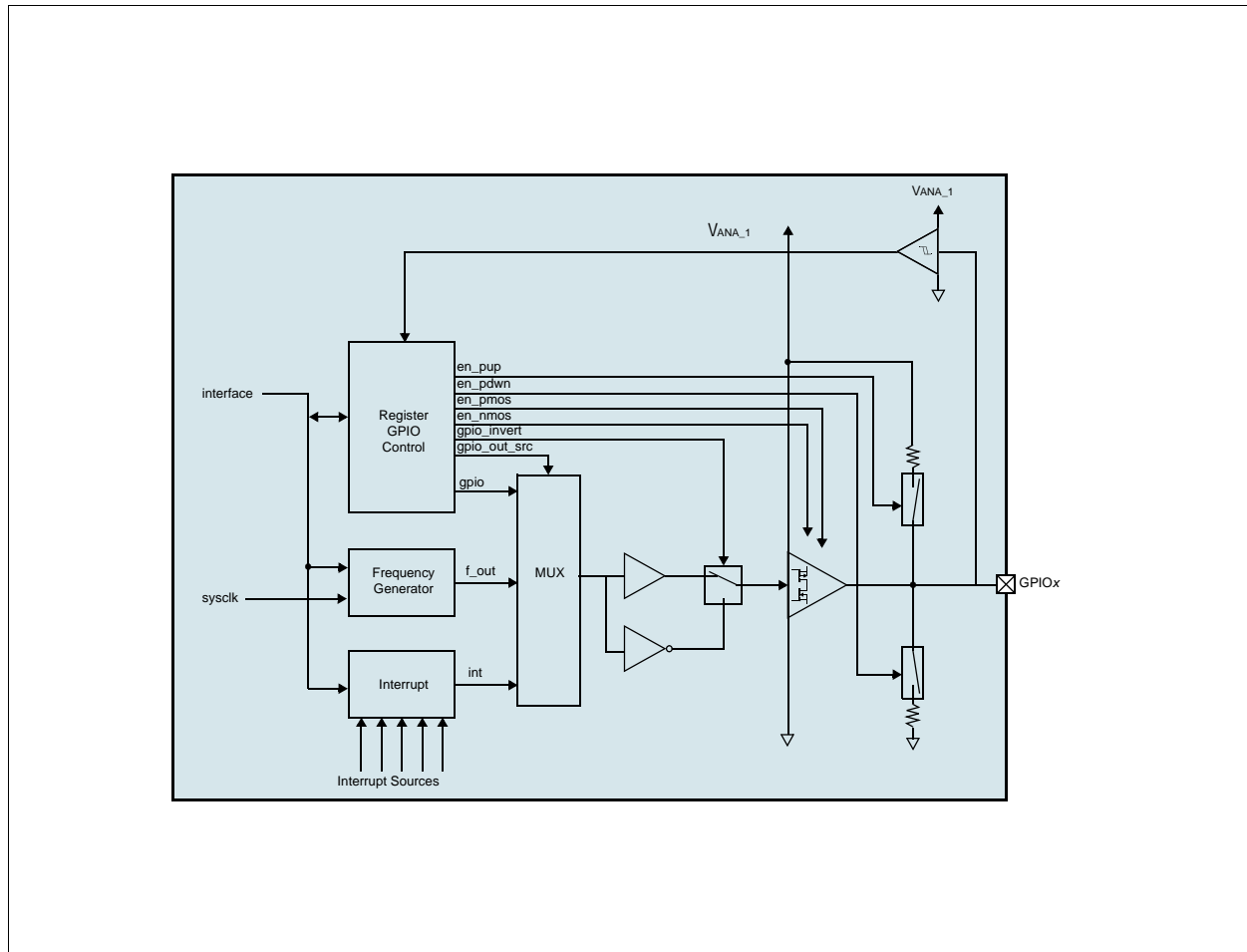
7.5.1 GPIO Registers

GPIO1 - GPIO3 are controlled by the registers listed in Table 17.

Table 17. GPIO Register Summary

Name	Addr.	b7	b6	b5	b4	b3	b2	b1	b0	Page
GPIO1 Control	1Ah	gpio1_out_src		gpio1_invert	gpio1_pulls		gpio1_low_curr	gpio1_mode		38
GPIO2 Control	1Bh	gpio2_out_src		gpio2_invert	gpio2_pulls		gpio2_low_curr	gpio2_mode		38
GPIO3 Control	1Ch	gpio3_out_src		gpio3_invert	gpio3_pulls		gpio3_low_curr	gpio3_mode		39
GPIO Signal	21h	-					gpio3	gpio2	gpio1	40
GPIO Frequency Control High Time	22h	gpio_h_time								41
GPIO Frequency Control Low Time	23h	gpio_l_time								41
Clock Generation	1Eh	-							ext_clk	41
Interrupt Enable	1Fh	chgov_int_en	chgrmv_int_en	resume_int_en	chdet_int_en	onkey_int_en	ovtmp_int_en	vchoff_int_en	wdog_int_en	42
Interrupt Status	20h	chgov_i	chgrmv_i	resume_i	chdet_i	onkey_i	ovtmp_i	vchoff_i	wdog_i	43

GPIO1 Control Register (Address 1Ah).

Addr: 1Ah		GPIO1 Control		
		Configures pin GPIO1.		
Bit	Bit Name	Default	Access	Bit Description
1:0	gpio1_mode	00	R/W	Sets the direction for pin GPIO1.
				00 Input only
				01 Output (push and pull)
				10 Output (open drain, only push; only NMOS is active)
				11 Output (open drain, only pull; only PMOS is active)
2	gpio1_low_curr	0	R/W	0 Fast output slew rate
				1 Slow output slew rate
4:3	gpio1_pulls	00	R/W	Sets pullup/pulldown to pin GPIO1 (independent of bit **gpio1_mode** setting).
				00 None
				01 Pulldown
				10 Pullup
				11 NA
5	gpio1_invert	0	R/W	0 Output signal is not inverted.
				1 Inverts any output signal going to GPIO1. This is useful for the Watchdog output source to make the output active high or low.
7:6	gpio1_out_src	00	R/W	Sets the source of pin GPIO1 output.
				x0 Bit **gpio1** controlled through the serial interface.
				01 Frequency generator defined by bits **gpio_h_time** and **gpio_l_time**.
				11 Interrupt signal (see Interrupt Function on page 42).

GPIO2 Control Register (Address 1Bh).

Addr: 1Bh		GPIO2 Control		
		Configures pin GPIO2.		
Bit	Bit Name	Default	Access	Bit Description
1:0	gpio2_mode	00	R/W	Sets the direction for pin GPIO*2.*
				00 Input only
				01 Output (push and pull)
				10 Output (open drain, only push; only NMOS is active)
				11 Output (open drain, only pull; only PMOS is active)
2	gpio2_low_curr	0	R/W	0 Fast output slew rate
				1 Slow output slew rate

Addr: 1Bh		GPIO2 Control		
		Configures pin GPIO2.		
Bit	Bit Name	Default	Access	Bit Description
4:3	gpio2_pulls	00	R/W	Sets pullup/pulldown to pin GPIO2 (independent of bit **gpio2_mode** setting).
				00	None
				01	Pulldown
				10	Pullup
				11	NA
5	gpio2_invert	0	R/W	0	Output signal is not inverted.
				1	Inverts any output signal going to pin GPIO2. This is useful for the Watchdog output source to make the output active high or low.
7:6	gpio2_out_src	00	R/W	Sets the source of pin GPIO2 output.
				x0	Bit **gpio2** (controlled through the serial interface).
				01	Frequency generator defined by bits **gpio_h_time** and **gpio_l_time**.
				11	Interrupt signal (see Interrupt Function on page 42).

GPIO3 Control Register (Address 1Ch).

Addr: 1Ch		GPIO3 Control		
		Configures pin GPIO3.		
Bit	Bit Name	Default	Access	Bit Description
1:0	gpio3_mode	00	R/W	Sets the direction for pin GPIO3.
				00	Input only.
				01	Output (push and pull).
				10	Output (open drain, only push; only NMOS is active).
				11	Output (open drain, only pull; only PMOS is active).
3:2	gpio3_low_curr	0	R/W	0	Fast output slew rate
				1	Slow output slew rate

Addr: 1Ch		GPIO3 Control			
		Configures pin GPIO3.			
Bit	Bit Name	Default	Access	Bit Description	
4	gpio3_pulls	00	R/W	Sets pullup/pulldown to pin GPIO3 (independent of bit **gpio3_mode** setting).	
				00	None
				01	Pulldown
				10	Pullup
				11	NA
5	gpio3_invert	0	R/W	0	Output signal is not inverted.
				1	Inverts any output signal going to pin GPIO3. This is useful for the Watchdog output source to make the output active high or low.
7:6	gpio3_out_src	00	R/W	Sets the source of pin GPIO3.	
				x0	Bit **gpio3** (controlled through the serial interface)
				01	Frequency generator defined by bits **gpio_h_time** and **gpio_l_time**.
				11	Interrupt signal (see Interrupt Function on page 42).

GPIO Signal Register (Address 21h).

Table 18. GPIO Signal Register (Address 33)

Addr: 21h		GPIO Signal		
		Reads the logic signal of the GPIO pins, independently of any other GPIO bit setting.		
Bit	Bit Name	Default	Access	Bit Description
0	gpio1	NA	R	Reads the logic signal from pin GPIO1. If **gpio1_out_src** = 00, this is the output signal at pin GPIO1.
1	gpio2	NA	R	Reads the logic signal from pin GPIO2. If **gpio2_out_src** = 00, this is the output signal at pin GPIO2.
2	gpio3	NA	R	Reads the logic signal from pin GPIO3. If **gpio3_out_src** = 00, this is the output signal at pin GPIO3.
7:3	-	NA	NA	

7.5.2   Programmable Frequency Generator

The Programmable Frequency Generator is controlled by bits **gpio_h_time** and **gpio_l_time**. It generates a waveform with 0.9 microseconds times **gpio_h_time** high-level and 0.9 microseconds times **gpio_l_time** low-level. The accuracy of these timings is ±10%.

The frequency of the Programmable Frequency Generator is:

$$f=1/(t_{CLK}*gpio\_h\_time + t_{CLK}*gpio\_l\_time) \qquad (EQ\ 1)$$

Where:
tclk = 1/f_{CLK} = 1/1.1MHz (typ) = 0.909μs (typ)

The purpose of the Programmable Frequency Generator is to have a controlled sweepable frequency or duty cycle source for one of the following:

- General User-Defined Clock

- 8-Bit DAC (output should be filtered by an RC filter)

- (High) Positive and Negative Voltage Generation

7.5.3   Programmable Frequency Generator Registers

Bit definition for programmable frequency generator registers are given below.

GPIO Frequency Control High Time Register (Address 22h).

Addr: 22h		GPIO Frequency Control High Time			
		Configures programmable frequency generator.			
Bit	Bit Name	Default	Access	Bit Description	
7:0	gpio_h_time	00$_h$	R/W	Defines the number of system clock cycles (typ 0.9μs), that the programmable frequency generator at the GPIO output(s) is high.	
				00$_h$	0.909μs
				FF$_h$	232.7μs

GPIO Frequency Control Low Time Register (Address 23h).

Addr: 23h		GPIO Frequency Control Low Time			
		Configures programmable frequency generator.			
Bit	Bit Name	Default	Access	Bit Description	
7:0	gpio_l_time	64$_h$	R/W	Defines the number of system clock cycles (typ 0.9μs), that the programmable frequency generator at the GPIO output(s) is low.	
				00$_h$	0.909μs
				FF$_h$	232.7μs

7.5.4   Interrupt Function

Any of the GPIO pins (GPIO1 - GPIO3) can be configured as interrupt output pins. To enable this function, the corresponding GPIO control bits must be set to 11b. See **gpio1_out_src**, **gpio2_out_src**, or **gpio3_out_src**.

Several signals can be configured as interrupt source using the Interrupt Enable (page 42). A rising edge of an enabled interrupt control signal sets the selected GPIO interrupt output pin = 1.

The Interrupt Status (page 43) shows the currently active interrupt signals. Reading this register resets the Interrupt Status (page 43) bits and sets the active GPIO pin (GPIO 1 - GPIO3) = 0.

7.5.5   Interrupt Registers

Bit definition for Interrupt registers are given below.

Interrupt Enable Register (Address 1Fh).

Addr: 1Fh		Interrupt Enable			
		Enables/disables interrupt sources.			
Bit	Bit Name	Default	Access		Bit Description
0	wdog_int_en	0	R/W	0	Disables watchdog alarm as interrupt source signal.
				1	Enables watchdog alarm as interrupt source signal.
1	vchoff_int_en	1	R/W	0	Disables charge termination voltage as interrupt source signal.
				1	Enables charge termination voltage as interrupt source signal.
2	ovtmp_int_en	1	R/W	0	Disables ov_temp_110 (device temperature alert at 110ºC).
				1	Enables ov_temp_110 (device temperature alert at 110ºC).
3	onkey_int_en	1	R/W	0	Disables pin ON (active high).
				1	Enables pin ON (active high).
4	chdet_int_en	1	R/W	0	Disables charger detection.
				1	Enables charger detection.
5	resume_int_en	1	R/W	0	Disables charger-resume interrupt.
				1	Enables charger-resume interrupt.
6	chgrmv_int_en	1	R/W	0	Disables charger-removed interrupt.
				1	Enables charger-removed interrupt.
7	chgov_int_en	1	R/W	0	Disables charger overvoltage interrupt.
				1	Enables charger overvoltage interrupt.

Interrupt Status Register (Address 20h).

Addr: 20h		Interrupt Status			
		Displays the status of the interrupt inputs.			
Bit	Bit Name	Default	Access	Bit Description	
0	wdog_i	0	R	0	Software or hardware watchdog is OFF or has not rolled over.
				1	Software or hardware watchdog is rollover.
1	vchoff_i	0	R	0	Battery voltage is below V$_{CHOFF}$ (see page 12) threshold.
				1	Battery voltage has reached V$_{CHOFF}$ threshold.
2	ovtmp_i	0	R	0	Device temperature is below 110ºC.
				1	110ºC temperature threshold **ov_temp_110** has been reached.
3	onkey_i	0	R	0	ON key has not been pressed.
				1	ON key has been pressed (rising edge).
4	chdet_i	0	R	Charger detection interrupt, active if **ChDet** is falling.	
5	resume_i	0	R	Active if V$_{RESUME}$ is reached (see Table 5).	
6	chgrmv_i	0	R	Charger detection interrupt, active if **ChDet** is falling.	
7	chgov_i	0	R	Charger over voltage interrupt, active if **ChOv** is rising.	

7.6 Current Sinks

The AS3605 contains 5 general purpose current sinks intended to control backlights, buzzers, and vibrators. All current sinks have an integrated protection (VPROTECT) against overvoltage and can therefore also drive inductive loads. The current sinks can also be used as switches to VSS with configurable impedance as indicated in Table 19.

Table 19. Current Source Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{CURRx}	curr1_current = 01_h - FF_h curr2_current = 01_h - FF_h	0.63		160	mA	resolution = 0.6275mA
I_{CURRx}	curr3_current = 01_h - FF_h curr4_current = 01_h - FF_h curr5_current = 01_h - FF_h	0.16		40	mA	resolution = 0.1569mA
VPROTECT	Maximum voltage at pin CURR*x* to protect driver transistor			V_{BAT} + 2.0V	V	$I_{SINK} \geq$ 20mA, guaranteed by design

Note: If a voltage higher than VPROTECT is applied to pins CURR1 - CURR5, a current of more than 20mA will flow into the AS3605. This protects the device from voltage rises caused by inductive loads.

7.6.1 Current Sink Registers

The current sinks are controlled by the registers listed in Table 20.

Table 20. Current Sink Register Summary

Name	Addr.	b7	b6	b5	b4	b3	b2	b1	b0	Page
CURR5 Control GPIO Map	19h			-		curr5_gpio		curr5_ctrl		45
CURR1 Value	24h	curr1_current								45
CURR2 Value	25h	curr2_current								45
CURR3 Value	26h	curr3_current								46
CURR4 Value	27h	curr4_current								46
CURR Control	28h	curr4_ctrl		curr3_ctrl		curr2_ctrl		curr1_ctrl		46
CURR5 Value	29h	curr5_current								47
CURR GPIO Map	2Ah	curr4_gpio		curr3_gpio		curr2_gpio		curr1_gpio		47

Note: For all current sinks, the currx_on signal is controlled with the currx_ctrl bits.

CURR5 Control GPIO Map Register (Address 19h).

Addr: 19h		CURR5 Control GPIO Map			
Bit	Bit Name	Default	Access	Bit Description	
1:0	curr5_ctrl	00b	R/W	00	Pin CURR5 is turned OFF
				01	Pin CURR5 is active
				1x	GPIO control; pin is active when **curr5_gpio** = 1
3:2	curr5_gpio	00b	R/W	If the bits **curr5_ctrl** = 1x, the following pin is assigned for turning the CURR5 pin ON and OFF.	
				00	GPIO1
				01	GPIO2
				10	GPIO3
				11	NA
7:4	-	NA	NA		

CURR1 Value Register (Address 24h).

Addr: 24h		CURR1 Value			
		Sets the current / resistance of current source CURR1.			
Bit	Bit Name	Default	Access	Bit Description	
7:0	curr1_current	00_h	R/W	00_h	Power Down
				01_h	0.6275mA
				…	
				FF_h	160mA

CURR2 Value Register (Address 25h).

Addr: 25h		CURR2 Value			
		Sets the current / resistance of current source CURR2.			
Bit	Bit Name	Default	Access	Bit Description	
7:0	curr2_current	00_h	R/W	00_h	Power Down
				01_h	0.6275mA
				…	
				FF_h	160mA

CURR3 Value Register (Address 26h).

Addr: 26h		CURR3 Value			
		Sets the current / resistance of current source CURR3.			
Bit	Bit Name	Default	Access	Bit Description	
7:0	curr3_current	00_h	R/W	00_h	Power Down
				01_h	0.1569mA
				…	
				FF_h	40mA

CURR4 Value Register (Address 27h).

Addr: 27h		CURR4 Value			
		Sets the current / resistance of current source CURR4.			
Bit	Bit Name	Default	Access	Bit Description	
7:0	curr4_current	00_h	R/W	00_h	Power Down
				01_h	0.1569mA
				…	
				FF_h	40mA

CURR Control Register (Address 28h).

Addr: 28h		CURR Control			
		Selects software/ hardware control of current sources.			
Bit	Bit Name	Default	Access	Bit Description	
1:0	curr1_ctrl	00b	R/W	00	Pin CURR1 is turned OFF.
				01	Pin CURR1 is active.
				1x	GPIO control; pin is active when **curr1_gpio** =1.
3:2	curr2_ctrl	00b	R/W	00	Pin CURR2 is turned OFF.
				01	Pin CURR2 is active.
				1x	GPIO control; pin is active when **curr2_gpio** =1.
5:4	curr3_ctrl	00b	R/W	00	Pin CURR3 is turned OFF.
				01	Pin CURR3 is active.
				1x	GPIO control; pin is active when **curr3_gpio** = 1.
7:6	curr4_ctrl	00b	R/W	00	Pin CURR4 is turned OFF.
				01	Pin CURR4 is active.
				1x	GPIO control; pin is active when **curr4_gpio** = 1.

CURR5 Value Register (Address 29h).

Addr: 29h				CURR5 Value	
				Sets the current.	
Bit	Bit Name	Default	Access	Bit Description	
7:0	curr5_current	00_h	R/W	00_h	Power Down
				01_h	0.1569mA
				…	
				FF_h	40mA

CURR GPIO Map Register (Address 2Ah).

| Addr: 2Ah				CURR GPIO Map	
				Selects GPIO pin to control current sources.	
Bit	Bit Name	Default	Access	Bit Description	
1:0	curr1_gpio	00	R/W	If bits **curr1_ctrl** = 1*x*, the following pin is assigned for turning the CURR1 pin ON and OFF.	
				00	GPIO1
				01	GPIO2
				10	GPIO3
				11	NA
3:2	curr2_gpio	00	R/W	If bits **curr2_ctrl** = 1*x*, the following pin is assigned for turning the CURR2 pin ON and OFF.	
				00	GPIO1
				01	GPIO2
				10	GPIO3
				11	NA
5:4	curr3_gpio	00	R/W	If bits **curr3_ctrl** = 1*x*, the following pin is assigned for turning the CURR3 pin ON and OFF.	
				00	GPIO1
				01	GPIO2
				10	GPIO3
				11	NA
7:6	curr4_gpio	00	R/W	If bits **curr4_ctrl** = 1*x*, the following pin is assigned for turning the CURR4 pin ON and OFF.	
				00	GPIO1
				01	GPIO2
				10	GPIO3
				11	NA

7.7 Audio Amplifier

The integrated Audio Amplifier provides real CD-quality audio and can be used as a headphone amplifier for portable devices. It is designed to meet the operational and power requirements of portable devices by delivering:

■ 1W_{RMS} continuous power into 8Ω differential at 5V supply

■ 2 x 50mW_{RMS} into 32Ω single-ended at 5V supply

The Audio Amplifier provides the following operational features:

■ Total harmonic distortion is less than 0.1% at 1kHz and the quiescent current does not exceed 8mA.

■ Power supply rejection is always better than 50dB and allows direct connection to noisy batteries, e.g. in TDMA systems.

■ The internal programmable gain can be used for volume and balance control.

■ Only a few external components are required for AC-coupling and reference bypass.

■ An internal smooth-rampup circuit ensures pop- and click-less startup without expensive and bulky external relays.

■ Device stability even with high capacitive loads of 1nF and does not require external snubber networks.

■ Inputs are high-impedance in power-down.

Figure 16. Audio Amplifier Block Diagram – Stereo Mode
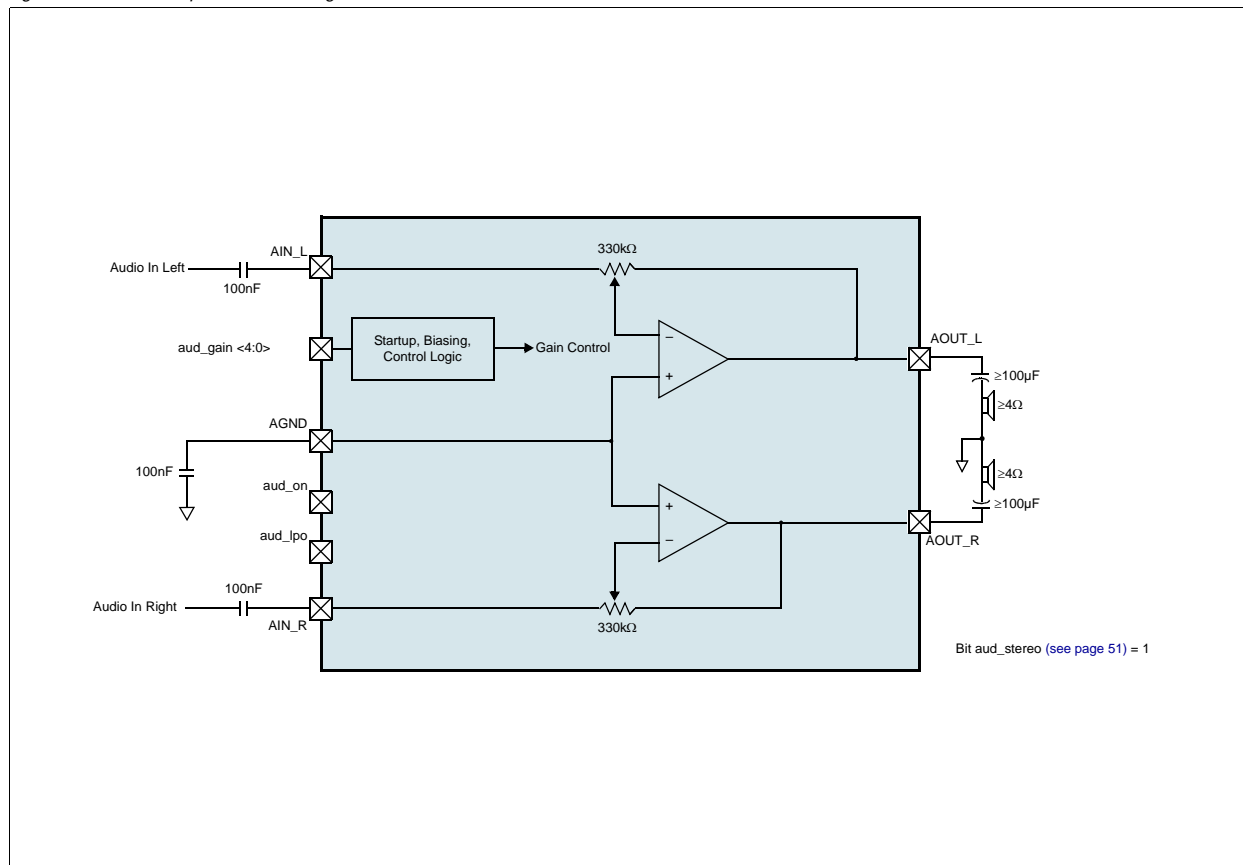
Note: The value of the audio output decoupling capacitors depends on the speaker impedance and the desired minimum output frequency:

$$C = 1/(2 x P x f x R) \hspace{3cm} (EQ\ 2)$$

Where:
f = minimum output cutoff frequency, -3dB point.
R = speaker impedance in Ω.
C = decoupling capacitance in F.

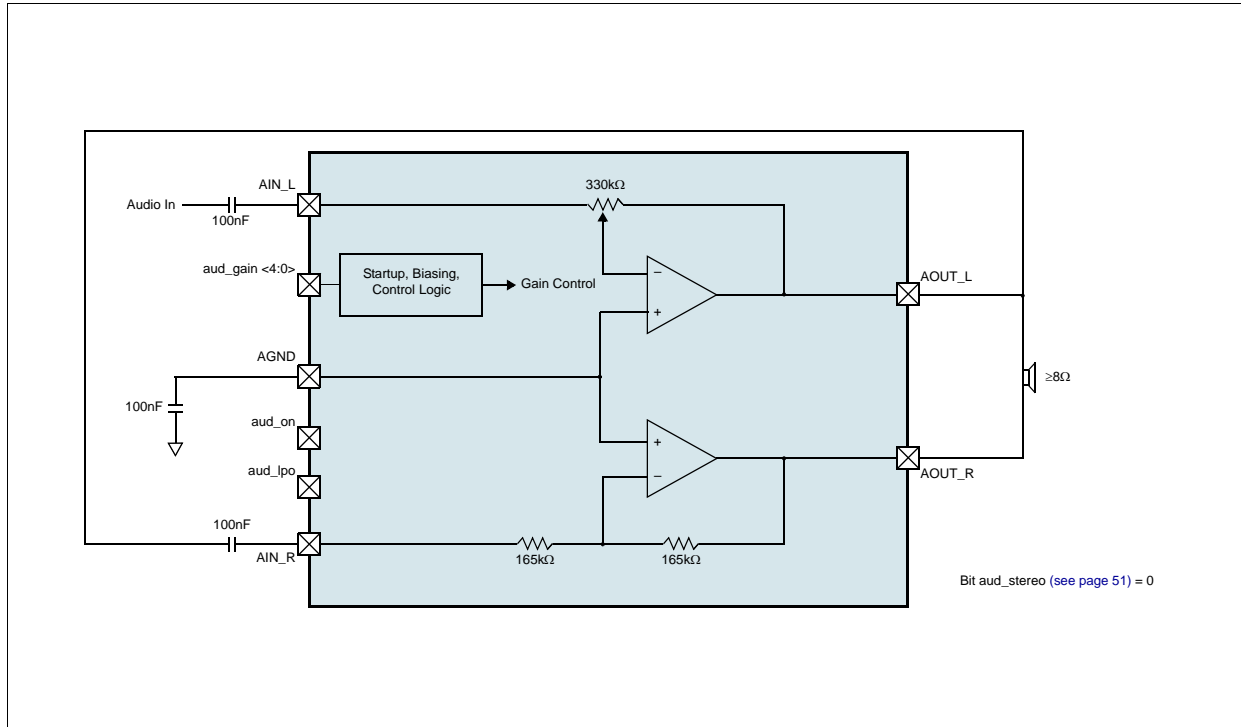*Figure 17. Audio Amplifier Block Diagram – Differential Mode*

Table 21. Audio Amplifier Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VDDH	Supply Voltage Range (VBAT_3)	3		5.5	V	
PSRR	Power Supply Rejection Ratio, Differential		70		dB	f = 1kHz
			50			f = 20kHz
PSRR	Power Supply Rejection Ratio, Single-Ended		50		dB	f = 1kHz
			40			f = 20kHz
IOFF	Shut Down Current			100	nA	
IVDDH	Supply Current (Differential Mode)			9	mA	**aud_lpo** = 0 and **aud_ib_red** = 00
				4		**aud_lpo** = 1 and **aud_ib_red** = 00
				2.7		**aud_lpo** = 1 and **aud_ib_red** = 11
IVDDH	Supply Current (Stereo Mode)			8	mA	**aud_lpo** = 0 and **aud_ib_red** = 00
				3		**aud_lpo** = 1 and **aud_ib_red** = 00
				1.7		**aud_lpo** = 1 and **aud_ib_red** = 11
RLOAD	Output Load	8			Ω	Differential mode
		4				Stereo mode
THD+N	Total Harmonic Distortion			0.1	%	POUT = 1W, RLOAD = 8Ω, f = 1kHz, VBAT = 5.5V; Differential
				0.5	%	POUT = 1W, RLOAD = 8Ω, f = 20kHz, VBAT = 5.5V; Differential
				0.05	%	POUT = 50mW, RLOAD =32Ω, f = 1kHz, VBAT = 4V; Single-Ended
				0.2	%	POUT = 50mW, RLOAD =32Ω, f = 20kHz, VBAT = 4V; Single-Ended

Table 21. Audio Amplifier Characteristics (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
SNR	Signal to Noise Ratio	84	91		dB	VBAT=3.7V, not tested, guaranteed per design
A0	Gain	-22	0	20	dB	Programmable gain: AOUT/AIN
ΔAx	Programmable Gain Step-Size		3		dB	
IOV_ON	Overcurrent On_limit	591	650	744	mA	Current rising into PMOS driver; when **aud_lpo** = 0 and **aud_ib_red** = 00, and **aud_overcur** = 1.
Iov_off	Overcurrent Off_limit	397	550	650	mA	Current decreasing in PMOS driver; when **aud_lpo** = 0 and **aud_ib_red** = 00, and **aud_overcur** is cleared.
Iov_hyst	Overcurrent Hysteresis		100		mA	

7.7.1 Audio Amplifier Registers

Bit definition for Audio amplifier registers are given below.

Audio Control Register (Address 2Bh).

Addr: 2Bh		Audio Control			
		Configures the Audio Amplifier.			
Bit	Bit Name	Default	Access	Bit Description	
0	aud_on	0	R/W	Activates the Audio Amplifier.	
				0	Audio amplifier off; inputs AIN_L and AIN_R are high-impedance.
				1	Audio amplifier on.
1	aud_lpo	0	R/W	Select Low-Power Operation; reduced output power.	
				0	Use for speakers < 32Ω (nominal impedance) in stereo mode; < 64Ω differential.
				1	Use for speakers ≥ 32Ω (nominal impedance) in stereo mode; ≥ 64Ω differential.
3:2	aud_ib_red	00b	R/W	Reduced bias current into Audio Amplifier circuit.	
				00	Use for speakers < 8Ω (nominal impedance) in stereo mode; < 16Ω differential.
				01	NA
				10	NA
				11	Use for speakers ≥ 8Ω (nominal impedance) in stereo mode; ≥ 16Ω differential.
7:4	aud_gain	0000b	R/W	Audio Amplifier gain adjust.	

Audio Amplifier gain adjust:

0000	Output off	1000	0dB
0001	-22dB	1001	+2dB
0010	-19dB	1010	+5dB
0011	-16dB	1011	+8dB
0100	-13dB	1100	+11dB
0101	-10dB	1101	+14dB
0110	-7dB	1110	+17dB
0111	-4dB	1111	+20dB

Audio Control 2 Register (Address 41h).

<table>
<tr><td rowspan="2">Addr: 41h</td><td colspan="4">Audio Control 2</td></tr>
<tr><td colspan="4">Configures the Audio Amplifier.</td></tr>
<tr><td>Bit</td><td>Bit Name</td><td>Default</td><td>Access</td><td colspan="2">Bit Description</td></tr>
<tr><td rowspan="3">0</td><td rowspan="3">aud_stereo</td><td rowspan="3">1</td><td rowspan="3">R/W</td><td colspan="2">Selects audio mode.</td></tr>
<tr><td>0</td><td>Differential mono mode (connect pin AIN_R to pin AOUT_L)</td></tr>
<tr><td>1</td><td>Stereo mode.</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">aud_overcur</td><td rowspan="2">0</td><td rowspan="2">R</td><td>0</td><td>Normal operation; audio output current below limit of IOV_ON.</td></tr>
<tr><td>1</td><td>Audio output current exceeds limit (IOV_ON).</td></tr>
<tr><td rowspan="5">3:2</td><td rowspan="5">aud_pulldwn</td><td rowspan="5">00b</td><td rowspan="5">R/W</td><td colspan="2">Audio amplifier output pulldown control; active if aud_on=0.</td></tr>
<tr><td>00</td><td>30µA</td></tr>
<tr><td>01</td><td>0.6mA</td></tr>
<tr><td>10</td><td>1.2mA</td></tr>
<tr><td>11</td><td>2.5mA</td></tr>
<tr><td>7:4</td><td>-</td><td>NA</td><td>Na</td><td colspan="2"></td></tr>
</table>

8 System Supervisory Functions

8.1 Reset

XRES is an active low bi-directional pin; an external pullup to LDO VANA_1 has to be added (see Digital Input/Output DC/AC Characteristics on page 61). During each reset cycle the following states are controlled by the AS3605:

- Pin XRES is Forced to GND

- Programmable Power-off Function

- Programmable Power-on Sequence and Regulator Voltages

- Programmable Reset Timer

- All Register bits Set to Default Values after Power-On (except the Audio Control 2 (page 51), the Interrupt Status (page 43).

Note: Programming is controlled by the internal OTP-ROM.

8.1.1 Reset Conditions

Reset can be activated from 7 different sources:

- Power On (Battery or Charger Insertion)

- Low Battery

- Power Off Mode

- Software Forced Reset

- Externally Triggered through the XRES Pin

- Overtemperature

- Watchdog

- Momentary Power Loss Detection

Power On (Battery or Charger Insertion). There are two types of voltage dependent resets:

- V_{POR} – Monitors the voltage on pin V2_5. LDO V2_5 uses the voltage $V_{CHARGER}$ or V_{BAT} as its source.

- V_{RESET} – Monitors the voltage on V_{BAT} pins. Pin XRES is only released if $V_{2\_5} > V_{POR}$ and $V_{BAT} > V_{RESETRISE}$.

Low Battery. A reset is automatically generated if V_{BAT} drops below $V_{RESETFALLING}$ for a minimum period ($V_{RESETMASK}$).

Table 22. Reset Levels

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{POR}	Overall power on reset	1.5	2.0	2.3	V	Monitor voltage on pin V2_5; power on reset for all internal functions. Pin RESET stays low until $V_{2\_5} > V_{POR}$
$V_{RESETRISE}$	Reset level for V_{BAT} rising		3.1		V	Monitor voltage on pin V_{BAT}; rising level.
$V_{RESETFALLING}$	Reset level for V_{BAT} falling[1]		2.8		V	Monitor voltage on pin V_{BAT}; falling level.
$V_{RESETMASK}$	Mask time for $V_{RESETFALLING}$		40		µs	Duration for $V_{BAT} < V_{RESETFALLING}$ until a reset cycle is started[2].
$T_{POWERLOSS}$	Interval for recovery of power loss on V_{BAT}	100	250	500	ms	If the duration of a power loss on V_{BAT} is below this duration, the system will restart

1. $V_{RESETFALLING}$ is only accepted if the reset condition is longer than $V_{RESETMASK}$. This guard time is used to avoid a complete reset of the system in case of short drops of V_{BAT}.

2. V_{RESET} signal is debounced with the specified mask time for rising- and falling-slope of V_{BAT}. The default time is 40µs and it can be programmed from 0µs to 200µs with the register reset-mask timer.

Power Off. Setting bit **power_off** = 1 puts the AS3605 into ultra low-power mode. To start a complete reset cycle, the AS3605 waits until the external pin ON is pulled high, the Battery Charger is inserted, or level V$_{POR}$ is reached. Bit **power_off** is automatically cleared by this reset cycle. During power off state, all circuits are turned off except LDO V2_5, thus the current consumption of the AS3605 is reduced to less than 10μA. The digital part is supplied by LDO V2_5, all other circuits are turned off in this mode, including internal references and oscillator.

Note: All registers except the Reset Control on page 53 are set to their default value after power-on.

Software Forced Reset. Setting bit **force_reset** = 1 immediately initiates a reset cycle, and is automatically cleared during a reset.

External Triggered Reset. If the pin XRES is pulled from high to low by an external source (microprocessor or button) a reset cycle is initiated.

Overtemperature Reset. The reset cycle can be started by overtemperature conditions (see page 55).

Watchdog Reset. If the Watchdog is armed (bit **wtdg_on** = 1 and bit **wtdg_res_on** = 1) and the timer expires, a reset is initiated. Refer to page 57 for information about the Watchdog block.

8.1.2 Reset Registers
Bit definition for Reset registers are given below.

Reset Control Register (Address 3Ah).

Addr: 3Ah		Reset Control		
		Controls reset and power off.		
Bit	Bit Name	Default	Access	Bit Description
0	force_reset	0	R/W	0	Normal operation.
				1	Initiates a complete reset cycle.
1	power_off	0	R/W	0	Normal operation.
				1	Initiates power-off mode where all LDOs are turned off except LDO V2_5. The AS3605 waits for a rising edge on pin ON or until the battery charger is detected.
2	on_input	0	R	Static indication of ON input pin.
				0	ON input pin is low.
				1	ON input pin is high (external ON key depressed).
5:3	reset_reason	0h	R	Indicates to the software the reason for the most recent reset.
				000	**VPOR** was reached (initial battery or charger insertion)
				001	**VRESETFALLING** was reached (V$_{BAT}$ < 2.75V)
				010	Software forced by bit **force_reset**
				011	Software forced by bit **power_off** and a Battery Charger detected
				100	Software forced by bit **power_off** and ON was pulled high
				101	Externally triggered through pin XRES
				110	Reset caused by overtemperature T140
				111	Reset caused by Watchdog
6	tmp_ pwr_loss	0	R	0	Normal startup.
				1	A momentary power loss condition was detected.
7	-	NA	NA		

Reset Timer Register (Address 13h).

Addr: 13h		Reset Timer			
		Sets the RESET timer value.			
Bit	Bit Name	Default	Access	Bit Description	
2:0	res_timer	OTP	R/W	Set RES$_{TIME}$	
				000	RES$_{TIME}$ = 0ms
				001	RES$_{TIME}$ = 10ms
				010	RES$_{TIME}$ = 20ms
				011	RES$_{TIME}$ = 30ms
				100	RES$_{TIME}$ = 40ms
				101	RES$_{TIME}$ = 50ms
				110	RES$_{TIME}$ = 60ms
				111	RES$_{TIME}$ = 70ms
5:3	reset_mask_timer	OTP	R/W	Set MASK$_{TIME}$	
				000	MASK$_{TIME}$ = 0µs
				001	MASK$_{TIME}$ = 5µs
				010	MASK$_{TIME}$ = 10µs
				011	MASK$_{TIME}$ = 40µs
				100	MASK$_{TIME}$ = 80µs
				101	MASK$_{TIME}$ = 120µs
				110	MASK$_{TIME}$ = 160µs
				111	MASK$_{TIME}$ = 200µs
7:6	-	NA	NA		

8.1.3   Reset Cycle

During a reset cycle, pin XRES is forced low for at least the time specified by bits **res_timer** and then all register bits are set to their default values except bit **ov_temp_140**.

During the reset time, a normal startup is initiated (refer to Startup on page 55) and the reset is active until the reset timer (set by bits **res_timer**) expires. The voltage on pin XRES is then pulled high by the external resistor and the whole system is leaving the reset state.

8.1.4   res_con: Reset Control

Reset is internally generated from a power on detection circuit (see page 52) and provided to the internal logic as well as externally through the open-drain pin XRES. This pin can also be forced externally by pulling it low. Additionally Reset can be forced by software by setting bit **force_reset** = 1.

8.2   Startup

8.2.1   Normal Startup

During a normal reset cycle (see page 52), after $V2\_5$ is above V_{POR} and V_{BAT} is above $V_{RESETRISE}$, a normal startup is initiated as follows:

1. The external capacitor on pin CREF is charged to 1.8V.

2. The DC/DC converters and LDOs are sequentially powered up according to the Boot OTP configuration.

3. Depending on the Boot OTP setting (Auto-Shutdown):
   a) The AS3605 enters shutdown mode if no momentary power loss is detected (only valid through initial start-up, not during a reset cycle).
   -or-
   b) The Reset-Timer is set by the Boot OTP and the reset is released when the Reset-Timer expires (pin XRES is pulled high).

8.2.2   Programmable Startup Sequences

The start-up sequnece is factory programmed. For more details please contact *austriamicrosystems* AG.

8.2.3   Startup from Battery Charger

If the voltage on pin VCHARGER is within $V_{STARTCHARGER}$, the Battery Charger is started in all cases, even with V_{BAT} = 0V. This allows the battery to be charged (even from deep discharge) and a normal startup to proceed.

Table 23. Battery Charger Startup Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{STARTCHARGER}$	Voltage on pin VCHARGER for the AS3605 to start	4.35	5.0	15	V	On pin VCHARGER.

8.3   Protection Functions

The Step Down DC/DC Converter, and all LDOs have integrated overcurrent protection. Overtemperature protection of the AS3605 is also built-in and can be activated with the serial interface bit **temp_pmc_on**.

The AS3605 has two temperature indicators:

■ **ov_temp_110** – Automatically reset if the overtemperature condition is removed.

■ **ov_temp_140** – Must be reset via the serial interface with bit **rst_ov_temp_140**. If **ov_temp_140** is set, an automatic reset of the complete AS3605 is initiated. Bit **ov_temp_140** is not cleared by this reset cycle to indicate the reason for this (unexpected) shutdown. It must be cleared intentionally by bit **rst_ov_temp_140**. The cause of this reset is stored in the Reset Control (page 53). This allows a detection of the reset cause, after the device has restarted.

8.3.1   TMP_SV: Temperature Supervision

The AS3605 includes an integrated temperature sensor, implemented to provide overtemperature protection of the device. It generates flags linked to the two temperature thresholds:

■ **T110** – 110º threshold. Sets **ov_temp_110**, signalling the 110º overtemperature condition. Thus software can react and shut down power-consuming functions in order to decrease the device's temperature.

■ **T140** – 140º threshold. Reaching this temperature level generates a Reset, when **temp_pmc_on** is enabled. This sets all regulators into power-down mode and stops battery charging.

8.3.2   Overtemperature Detection

Table 24. Overtemperature Detection Parameters

Symbol	Parameter	Min	Typ	Max	Unit
T_{110}	**ov_temp_110** Rising Threshold	95	110	125	ºC
		203	230	257	ºF
T_{140}	**ov_temp_140** Rising Threshold	125	140	155	ºC
		257	284	311	ºF
T_{hyst}	**ov_temp_110** and **ov_temp_140** Hysteresis		5		ºC

8.3.3   Overtemperature Detection Register

Overtemperature Control Register (Address 3Bh).

Addr: 3Bh		Overtemperature Control				
		Device temperature supervision.				
Bit	Bit Name	Default	Access	Bit Description		
0	temp_pmc_on	0	R/W	Activates/deactivates temperature supervision. Default: Off - all other bits are only valid if set to 1.		
				0	Temperature supervision is disabled. No reset will be generated when the device temperature exceeds 140ºC.	
				1	Temperature supervision is enabled.	
1	ov_temp_110	0	R	1	Warning flag indicating that the device temperature has exceeded 110ºC.	
2	ov_temp_140	0	R	1	Indicates that the device overtemperature has exceeded 140ºC. This bit is not cleared by the automatic reset caused by this flag. It must be cleared using bit **rst_ov_temp_140**.	
3	rst_ov_temp_140	0	R/W	Used to clear bit **ov_temp_140**; first set this bit = 1 and then set it =0.		
4	temp_test0	0	R/W	Only used for production; must always be set to 00.		
5	temp_test1	0	R/W			
6	tco_110_a	0	R	Only used for production – direct output of T110 comparator.		
7	tco_140_a	0	R	Only used for production – direct output of T140 comparator.		

8.4 Watchdog Block

The AS3605 includes a Watchdog block to detect a deadlock of the connected controller.

If the Watchdog block is active (**wtdg_on** = 1), it must get a continuous trigger signal within a programmable timer window. If there is no signal for a certain time period from a defined GPIO pin or bit **wtdg_sw_sig**, the Watchdog block starts either a complete reset – bit **wtdg_res_on** must be set to 1 – or sets interrupt flag **wdog_i**.

The Watchdog timer window is defined by bits:

- **wtdg_min_timer**

- **wtdg_max_timer**

The trigger signal can be configured using bits:

- **wtdg_trigger**

- **wtdg_sw_sig** – Watchdog is reset by software

- **wtdg_gpio_input** – Watchdog is reset by hardware (GPIO)

Any of the general purpose input/outputs can be configured as inputs using bit **wtdg_gpio_input**, and outputs using bits **gpio1_out_src**, **gpio2_out_src**, or **gpio3_out_src** = 11, for the Watchdog. While the GPIO input must be continuously re-triggered in order to avoid a Watchdog interrupt, the GPIO output will generate in interrupt when the Watchdog runs over – **wdog_int_en**.

8.4.1 Watchdog Registers

The Watchdog is controlled by the registers listed in Table 25.

Table 25. Low Dropout Regulators Register Summary

Name	Addr	b7	b6	b5	b4	b3	b2	b1	b0	Page
Watchdog Control	2Eh		-		wtdg_ trigger	wtdg_gpio_input		wtdg_ res_on	wtdg_on	57
Watchdog_min Timer	2Fh	wtdg_min_timer								58
Watchdog_max Timer	30h	wtdg_max_timer								58
Watchdog Software Signal	31h	-							wtdg_ sw_sig	58

Watchdog Control Register (Address 2Eh).

Addr: 2Eh		Watchdog Control			
		Controls the Watchdog block.			
Bit	Bit Name	Default	Access	Bit Description	
0	wtdg_on	0	R/W	0	Disables the Watchdog block.
				1	Enables the Watchdog block.
1	wtdg_res_on	1	R/W	If the Watchdog expires and this bit = 1, a reset cycle will be started. Refer to page 52 for information about reset cycles.	
				0	A watchdog overflow does not generate a reset.
				1	A watchdog overflow generates a reset.

Addr: 2Eh		Watchdog Control			
		Controls the Watchdog block.			
Bit	Bit Name	Default	Access	Bit Description	
3:2	wtdg_gpio_input	00	R/W	Specifies the input pin of the Watchdog if bit **wtdg_trigger** = 1.	
				00	GPIO1
				01	GPIO2
				10	GPIO3
				11	Do not use this setting.
4	wtdg_trigger	0	R/W	Select type of trigger (software or hardware).	
				0	Use bit **wtdg_sw_sig** as trigger signal for the Watchdog.
				1	Use the pin defined by bit **wtdg_gpio_input** as trigger signal for the Watchdog.
7:5	-	NA	NA		

Watchdog_min Timer Register (Address 2Fh).

Addr: 2Fh		Watchdog_min Timer			
		Sets the minimum Watchdog trigger time.			
Bit	Bit Name	Default	Access	Bit Description	
7:0	wtdg_min_timer	00_h	R/W	00_h	0s
				01_h	16ms
				…	
				FF_h	4.08s

Watchdog_max Timer Register (Address 30h).

Addr: 30h		Watchdog_max Timer			
		Sets the maximum Watchdog trigger time.			
Bit	Bit Name	Default	Access	Bit Description	
7:0	wtdg_max_timer	FF_h	R/W	01_h	16ms
				…	
				FF_h	4.08s
				Caution: Do not set these bits = 00_h	

Watchdog Software Signal Register (Address 31h).

Addr: 31h		Watchdog Software Signal			
		Resets the Watchdog block by software.			
Bit	Bit Name	Default	Access	Bit Description	
0	wtdg_sw_sig	0	R/W	Trigger input by the serial interface if **wtdg_trigger** = 0	
				0	Force watchdog trigger = low (see Figure 18)
				1	Force watchdog trigger = high (see Figure 18)
7:1	-	NA	NA		

Figure 18. Watchdog Timing Diagram
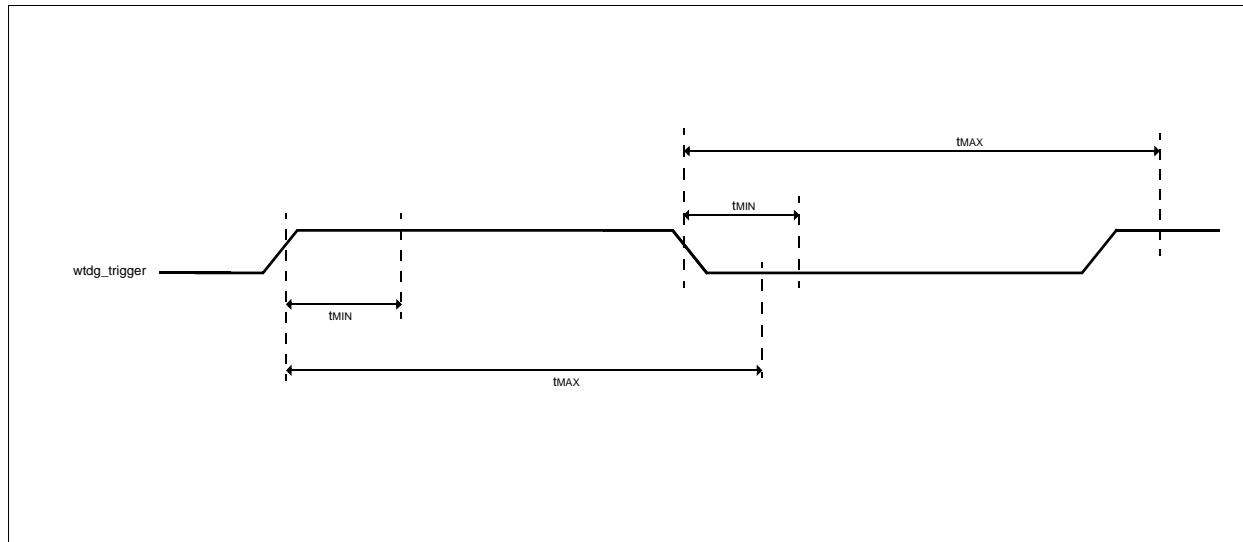
8.5 Internal Reference Circuits

The internal reference circuits (V, I, fCLK) require the external components listed in Table 26.

Table 26. Reference External Components

Symbol	Parameter	Min	Typ	Max	Unit	Notes
CEXT	External filter capacitor	-20%	100	+20%	nF	Ceramic low-ESR capacitor between pins CREF and VSS

Table 27. References Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VCEXT	Reference voltage	-1%	1.8	+1%	V	Low noise trimmed voltage reference - connected to pin CREF; do not load.
fCLK	Internal reference clock	1.0	1.1	1.2	MHz	Trimmed clock reference

To reduce the current consumption of the AS3605, internal references circuits can be set into a special low-power mode with bit **low_power_on**.

8.5.1   Internal Reference Registers

References Control Register (Address 2Dh).

Addr: 2Dh		References Control			
		Configures low-power mode.			
Bit	Bit Name	Default	Access	Bit Description	
0	low_power_on	0	R/W	0	Standard mode or controlled by GPIO, if **low_power_gpio_on** = 1.
				1	Low-power mode; all parameters except noise (see LDO parameters, section 7.3) are still valid.
1	low_power_gpio_on	0	R/W	If set and **low_power_on** = 0 then the low-power mode is controlled by a GPIO pin.	
				0	Low-power mode disabled for GPIO control.
				1	Low-power mode is activated by GPIO pin (**low_power_gpio**). **low_power_on** must be enabled.
3:2	low_power_gpio	00	R/W	Specifies the pin to be used as GPIO control.	
				00	GPIO1
				01	GPIO2
				10	GPIO3
				11	GPIO3
4	low_power_gpio_pol	0	R/W	0	Low-power mode is activated. If the selected GPIO input, bit **low_power_gpio** = 1.
				1	Low-power mode is activated. If the selected GPIO input, bit **low_power_gpio** = 0.
7:5	-	NA	NA		

8.6 Low Power Mode

Bit **low_power_on** controls low-power mode. In low-power mode the integrated voltage reference and the temperature supervision comparators operate in pulsed mode. This reduces the quiescent current of the AS3605 by 45µA (typical). Because of the pulsed function, the LDO output noise parameters do not meet the specification in low-power mode but the full functionality is still available.

Note: Low-power mode can be activated by hardware using one of the GPIO pins, or by software by setting bit **low_power_on** = 1.

8.7   Serial Interface

8.7.1   Digital Input/Output DC/AC Characteristics

VBAT_1 is used as supply voltage of the pins.

Table 28. DC Characteristics Input Pin SCK

Symbol	Parameter	Min	Max	Unit	Notes
V_{IH}	High-Level Input Voltage	1.5	V_{BAT}	V	
V_{IL}	Low-Level Input Voltage		0.4	V	
I_{LEAK}	Input Leakage Current	-5	5	µA	to VBAT_1 and GND_PAD

Table 29. DC Characteristics Open Drain Pin SDA

Symbol	Parameter	Min	Max	Unit	Notes
V_{IH}	High-Level Input Voltage	1.5		V	
V_{IL}	Low-Level Input Voltage		0.4	V	
I_{LEAK}	Input Leakage Current	-5	5	µA	to VBAT_1 and GND_PAD
V_{OL}	Low-Level Output Voltage		0.2	V	at 4.0mA
C_{LOAD}	Capacitive Load		50	pF	

Table 30. DC Characteristics Input/Output Open Drain Pin XRES

Symbol	Parameter	Min	Max	Unit	Notes
V_{IH}	High-Level Input Voltage	1.5		V	
V_{IL}	Low-Level Input Voltage		0.4	V	
I_{LEAK}	Input Leakage Current	-5	5	µA	to VANA_1 and GND_PAD
V_{OL}	Low-Level Output Voltage		0.2	V	at 4mA
C_{LOAD}	Capacitive Load		50	pF	
R_{PULLUP}	External Pullup Resistor		100k	Ω	Connect to <=VBAT_1

8.7.2   I^{2}C Compatible Serial Interface

The following pins are used for the I^{2}C interface:

■   SDA = I/O Pin

■   SCK = Input Pin

I^{2}C Features. Listed below are I^{2}C features:

■   Fast-mode capability (max. SCL-frequency is 400 kHz @ 100pF capacitive load)

■   7-bit addressing mode

■   Write formats:Single-Byte-Write, Page-Write

■   Read formats:Current-Address-Read, Random-Read, Sequential-Read

■   SDA input delay and SCL spike filtering by integrated RC-components

I^{2}C Slave Addresses. The AS3605 device address is fixed at 82$_h$ for write commands and 83$_h$ for read commands.

Figure 19.   Complete Data Transfer
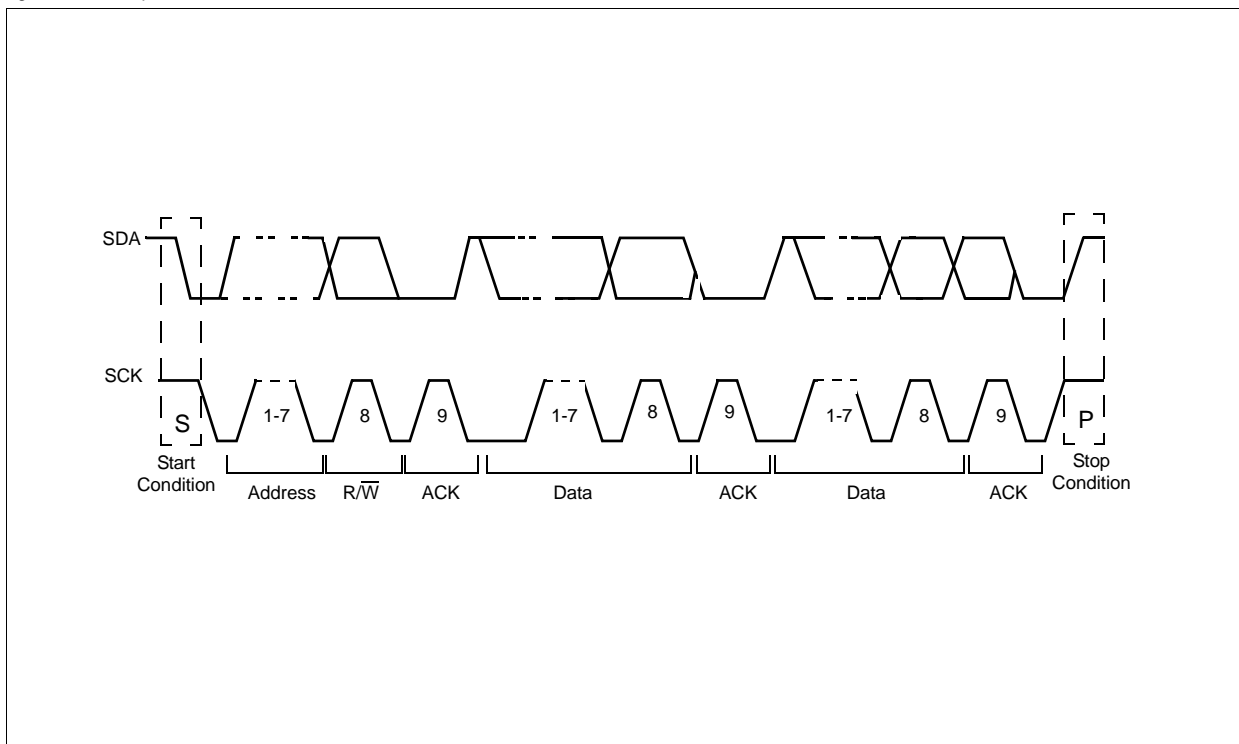
I²C Data Transfer Formats. Definitions used in the serial data transfer format diagrams (Figures 20 - 24) are listed in Table 31.

Table 31. I²C Data Transfer Byte Definitions

Symbol	Definition	R/W (AS3605 Slave)	Notes
S	Start condition after stop	R	1 bit
Sr	Repeated start	R	1 bit
DW	Device address for write	R	1000 0010 (82_h)
DR	Device address for read	R	1000 0011 (83_h)
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No acknowledge	R	1 bit
reg_data	Register data/write	R	8 bit
data (n)	Register data/read	R	1 bit
P	Stop condition	R	8 bit
WA++	Increment word address internally	R	During acknowledge

Figure 20. I²C Byte Write
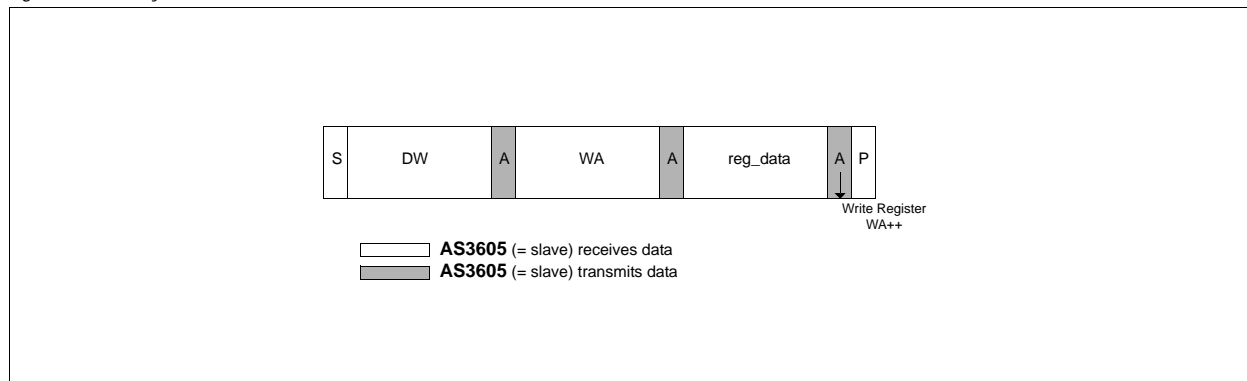
Figure 21. I²C Page Write
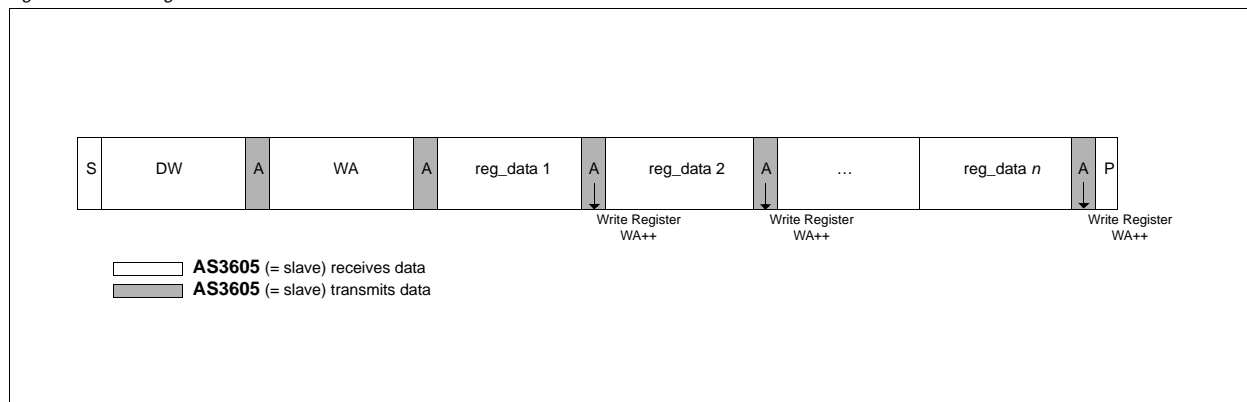
Byte Write and Page Write formats are used to write data to the slave.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

The following diagrams show some of the serial read formats supported by the AS3605.

Figure 22. I^2C Random Read
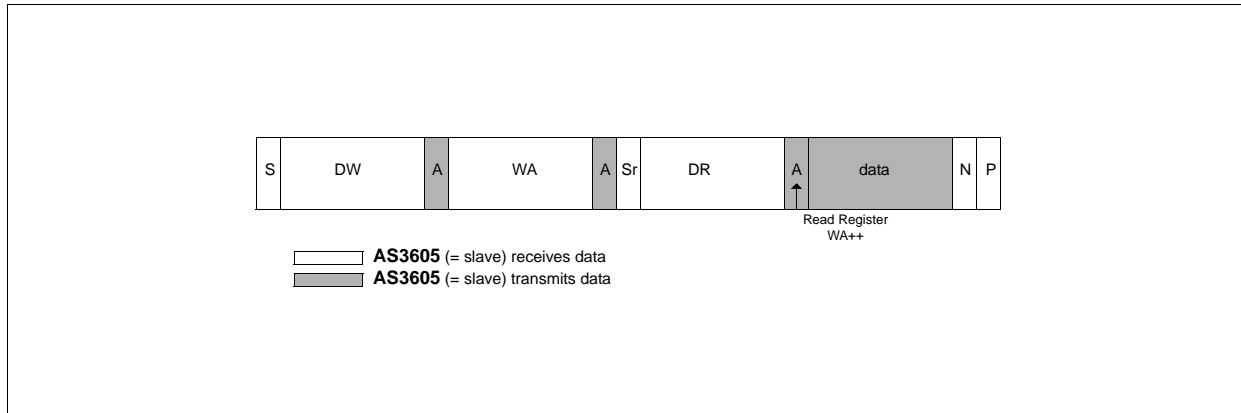
Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

Figure 23. I^2C Sequential Read
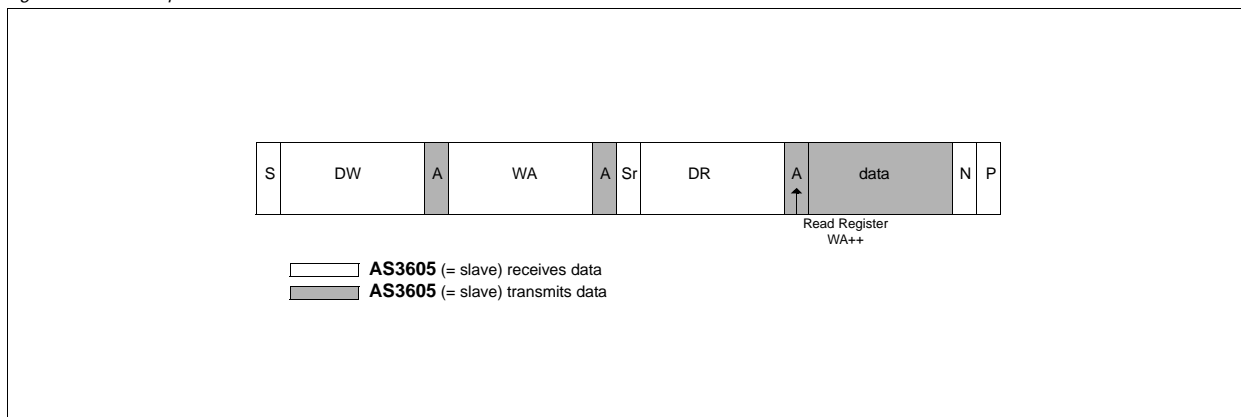
Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

Figure 24. I²C Current Address Read
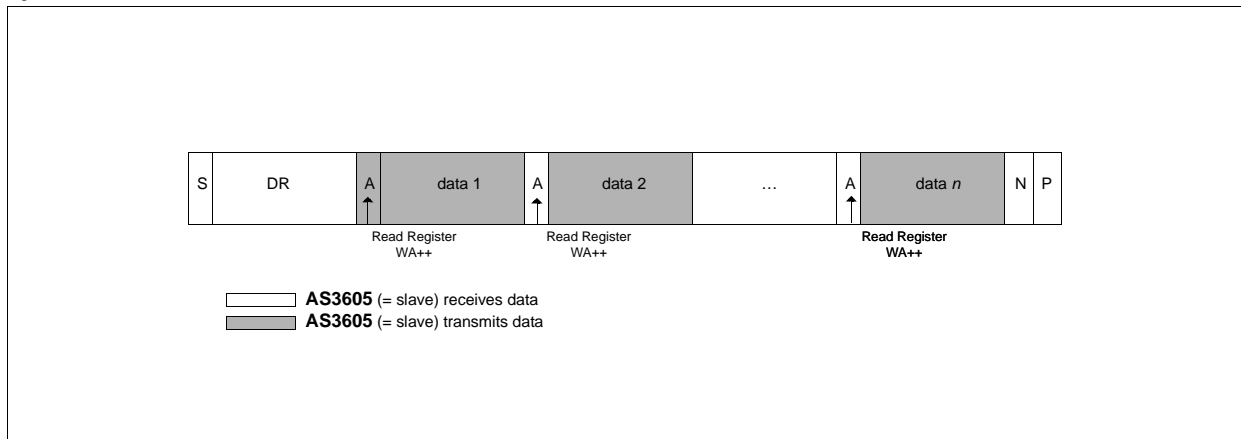
To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

9 Register Map

The AS3605 registers along with their addresses and default values are listed in Table 32. Fields marked NA are not used; reading these bits may result in 0s or 1s. Always use 0s, when writing to these bits.

Caution: Do not write to addresses not listed in Table 32.

Table 32. Register Summary

Register	Addr	Default	b7	b6	b5	b4	b3	b2	b1	b0
Step Down Voltage/ Test Modes	01h	00h	-		buck_v					
LDO_RF1 Voltage	02h	00h	-			ldo_rf1_v				
LDO_RF2 Voltage	03h	00h	-			ldo_rf2_v				
LDO_RF3 Voltage	04h	00h	-			ldo_rf3_v				
LDO_RF4 Voltage	05h	00h	-			ldo_rf4_v				
LDO_ANA2_Voltage	06h	00h	-			ldo_ana2_v				
LDO_ANA1_Voltage	07h	00h	-			ldo_ana1_v				
LDO_SIM_Voltage	08h	00h	NA	ldo_sim_v	-					
Reg Power	09h	00h	-		buck_on	ldo_sim_on	-	-	ldo_ana2_on	ldo_ana1_on
LDO_GPIO Active	0Fh	00h	-	-	ldo_rf4_gpio	ldo_rf3_gpio	Ldo_rf2_gpio	ldo_rf1_gpio	ldo_ana2_gpio	buck_gpio
LDO_RF Switch	10h	00h	ldo_rf4_on	ldo_rf3_on	ldo_rf2_on	ldo_rf1_on	EOCCurrent[1:0]		ana2_sw	ana1_sw
LDO_AD GPIOx	11h	00h	-				ldo_ana2_gpio_sel		buck_gpio_sel	
LDO_RF GPIOx	12h	00h	ldo_rf4_gpio_sel		ldo_rf3_gpio_sel		ldo_rf2_gpio_sel		ldo_rf1_gpio_sel	
Reset Timer	13h	00h	-		reset_mask_timer			res_timer		
ChargerControl1	14h	EDh	ChOvEn	TrickleCurrent[1:0]		ConstantCurrent[3:0]				ChEn
ChargerControl2	16h	58h	ChOv	ChOvH	-	Li4v2	resume_disable	-		
Step Down Config	17h	00h	buck_dis_curmin	buck_dis_pon	buck_lpo	-	-	buck_dis_n	buck_nsw_on	buck_psw_on
Charge Pump Control Onkey Pulldown	18h	00h	cp_auto_on	cp_start_debounce	onkey_pulld_off	cp_freq	cp_mode_switching	cp_mode[1:0]		cp_on
CURR5 Control GPIO Map	19h	00h	-					curr5_gpio	curr5_ctrl	
GPIO1 Control	1Ah	00h	gpio1_out_src		gpio1_invert	gpio1_pulls		gpio1_low_curr	gpio1_mode	
GPIO2 Control	1Bh	00h	gpio2_out_src		gpio2_invert	gpio2_pulls		gpio2_low_curr	gpio2_mode	
GPIO3 Control	1Ch	00h	gpio3_out_src		gpio3_invert	gpio3_pulls		gpio3_low_curr	gpio3_mode	
Interrupt Enable	1Fh	FEh	chgov_int_en	chgrmv_int_en	resume_int_en	chdet_int_en	onkey_int_en	ovtmp_int_en	eoc_int_en	wdog_int_en
Interrupt Status	20h	NA	chgov _i	chgrmv_i	resume_i	chdet_i	onkey_i	ovtmp_i	eoc_i	wdog_i
GPIO Signal	21h	NA	-					gpio3	gpio2	gpio1

Table 32. Register Summary

Register	Addr	Default	b7	b6	b5	b4	b3	b2	b1	b0
GPIO Frequency Control High Time	22h	00h	gpio_h_time							
GPIO Frequency Control Low Time	23h	00h	gpio_l_time							
CURR1 value	24h	00h	curr1_current							
CURR2 value	25h	00h	curr2_current							
CURR3 value	26h	00h	curr3_current							
CURR4 value	27h	00h	curr4_current							
CURR control	28h	00h	curr4_ctrl		curr3_ctrl		curr2_ctrl		curr1_ctrl	
CURR5 value	29h	00h	curr5_current							
CURR GPIO map	2Ah	00h	curr4_gpio		curr3_gpio		curr2_gpio		curr1_gpio	
Audio Control	2Bh	00h	aud_gain				aud_ib_red		aud_lpo	aud_on
References Control	2Dh	00h	NA			low_power_gpio_pol	low_power_gpio		low_power_gpio_on	low_power_on
Watchdog Control	2Eh	02h	NA			wtdg_trigger	wtdg_gpio_input		wtdg_res_on	wtdg_on
Watchdog_min Timer	2Fh	00h	wtdg_min_timer							
Watchdog_max Timer	30h	FFh	wtdg_max_timer							
Watchdog Software Signal	31h	00h	NA							wtdg_sw_sig
ChargerStatus	35h	NA	-	NoBat	EOC	CVM	Trickle	-	ChAct	ChDet
CP Mode Switch	36h	NA	-			curr5_on_cp	curr4_on_cp	curr3_on_cp	curr2_on_cp	curr1_on_cp
Curr Low Voltage Status	37h	NA	-			curr5_low_volt	curr4_low_volt	curr3_low_volt	curr2_low_volt	curr1_low_volt
Reset Control	3Ah	0h	NA	tmp_pwr_loss	reset_reason			on_input	power_off	force_reset
Overtemperature Control	3Bh	00h	tco_140_a	tco_110_a	temp_test1	temp_test0	rst_ov_temp_140	ov_temp_140	ov_temp_110	temp_pmc_on
ASIC ID 1	3Dh	33h	0	0	1	1	0	0	1	1
ASIC ID 2	3Eh	53h	Rev							
Audio Control 2	41h	0h	-				aud_pulldwn		aud_overcurr	aud_stereo

Read Only

10 External Parts List

The recommended specifications for external components (refer to Figure 1 and Figure 2) are listed below.

Table 33. External Parts Specification

Part	Min	Typ	Max	Tol. Min	Rating Min	Remarks	Package Min
C2		470nF		±20%	6.3V	Ceramic, X5R (Charge Pump)	0603
C3	1µF		4.7µF	±20%	6.3V	Ceramic, X5R (V5_6)	0603
C4	1µF		4.7µF	±20%	6.3V	Ceramic, X5R (VANA_1)	0603
C5		1µF		±20%	6.3V	Ceramic, X5R (VBAT_1)	0603
C6	1µF		4.7µF	±20%	6.3V	Ceramic, X5R (VANA_2)	0603
C7	1µF		2.2µF	±20%	6.3V	Ceramic, X5R (V2_5)	1206
C8	1µF		4.7µF	±20%	6.3V	Ceramic, X5R (VRF_1)	0603
C9		1µF		±20%	6.3V	Ceramic, X5R (VBAT_4)	0603
C10	1µF		4.7µF	±20%	6.3V	Ceramic, X5R (VRF_2)	0603
C11	1µF		4.7µF	±20%	6.3V	Ceramic, X5R (VRF_3)	0603
C13	1µF		4.7µF	±20%	6.3V	Ceramic, X5R (VRF_4)	0603
C16		1µF		±20%	6.3V	Ceramic, X5R (VBAT_2)	0603
C18		10µF		±20%	6.3V	Ceramic, X5R (VBUCK)	
C19		100nF		±20%	6.3V	Ceramic, X5R (VSIM)	0402
C20		100µF		±20%	6.3V	Tantalum; L Stereo Decoupling Cap.	
C21		100µF		±20%	6.3V	Tantalum; R Stereo Decoupling Cap.	
C22		1µF		±20%	6.3V	Ceramic, X5R (VBAT_3)	0603
C23		100nF		±20%	6.3V	Ceramic, X5R (Decoupling, AIN_L)	0402
C24		100nF		±20%	6.3V	Ceramic, X5R (Decoupling, AIN_R)	0402
C25		100nF		±20%	6.3V	Ceramic, X5R (AGND)	0402
C26	1µF		4.7µF	±20%	6.3V	Ceramic, X5R (VCHARGER)	0603
C27	10µF			±20%	6.3V	X5R; all VBAT Caps. Combined	0603
C29		100nF		±20%	6.3V	Ceramic, X5R (CREF)	0402
R4	50mΩ	100mΩ	150mΩ	±1%		Shunt resistor	0603
R5		100k		±10%		Reset Pullup Resistor	0201
L2		2.2µH		±20%		Recommended type: Coiltronics SD-12-2R2	
Q1	PBSS301PD or similar					Charger Transistor	

11 Package Drawings and Markings
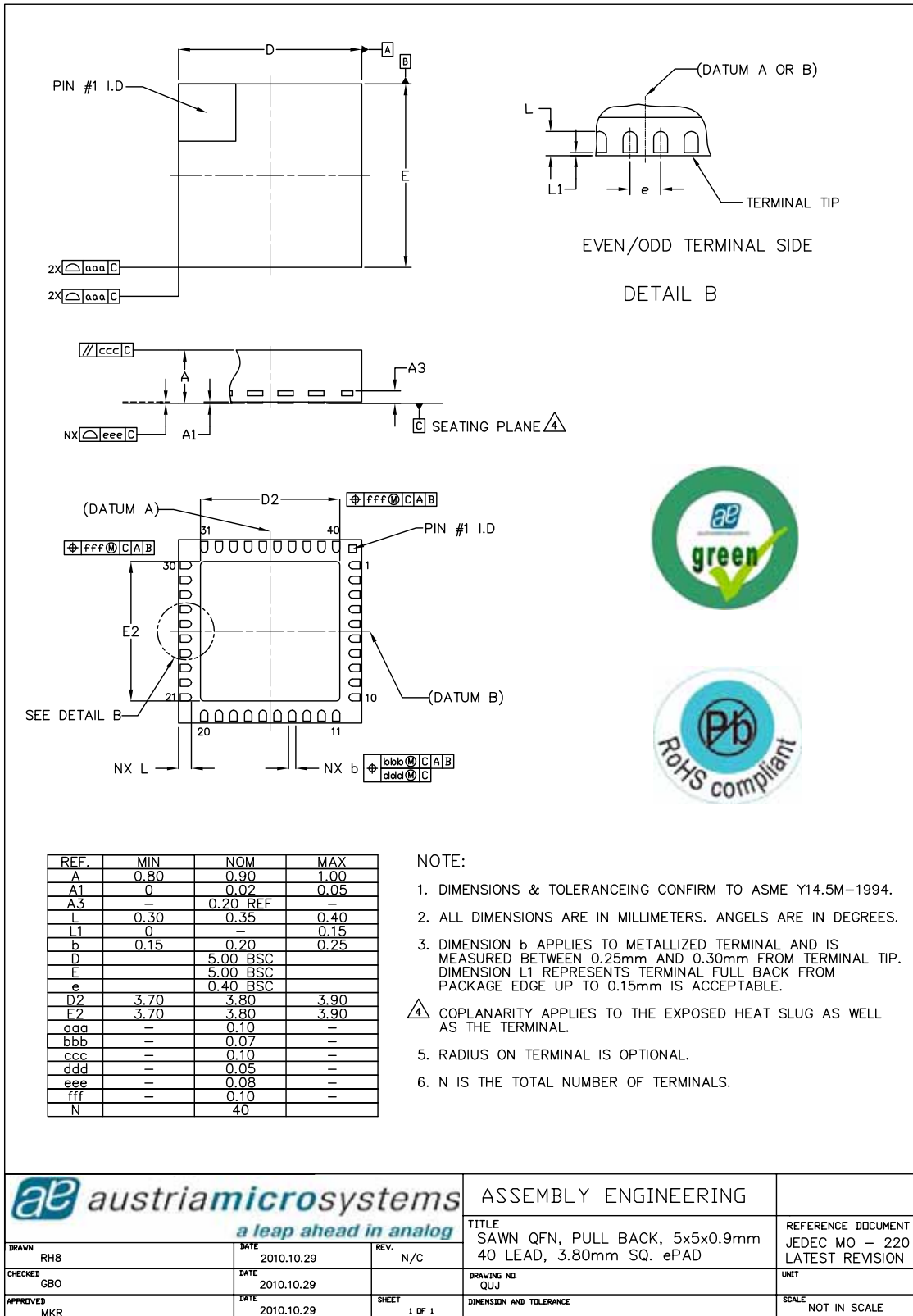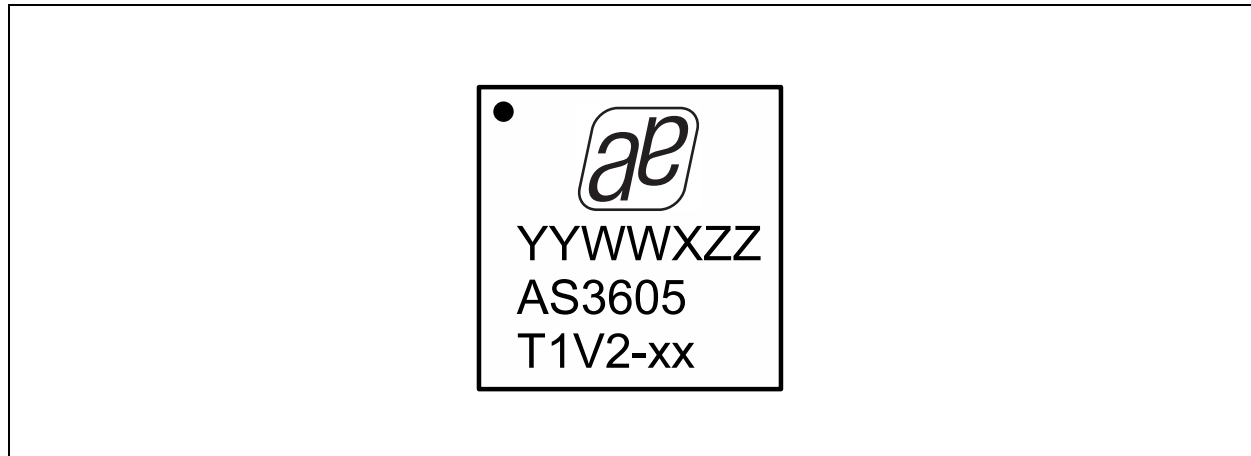
Figure 25. QFN40 (5x5mm) Drawings and Dimensions

REF.	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	–	0.20 REF	–
L	0.30	0.35	0.40
L1	0	–	0.15
b	0.15	0.20	0.25
D		5.00 BSC	
E		5.00 BSC	
e		0.40 BSC	
D2	3.70	3.80	3.90
E2	3.70	3.80	3.90
aaa	–	0.10	–
bbb	–	0.07	–
ccc	–	0.10	–
ddd	–	0.05	–
eee	–	0.08	–
fff	–	0.10	–
N		40	

NOTE:

1. DIMENSIONS & TOLERANCEING CONFIRM TO ASME Y14.5M−1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.

3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.15mm IS ACCEPTABLE.

4. COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

5. RADIUS ON TERMINAL IS OPTIONAL.

6. N IS THE TOTAL NUMBER OF TERMINALS.

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	TITLE SAWN QFN, PULL BACK, 5x5x0.9mm 40 LEAD, 3.80mm SQ. ePAD	**REFERENCE DOCUMENT** JEDEC MO − 220 LATEST REVISION
DRAWN RH8 **DATE** 2010.10.29 **REV.** N/C	**DRAWING NO.** QUJ	**UNIT**
CHECKED GBO **DATE** 2010.10.29		
APPROVED MKR **DATE** 2010.10.29 **SHEET** 1 OF 1	**DIMENSION AND TOLERANCE**	**SCALE** NOT IN SCALE

Figure 26. QFN Marking

Table 34. Package Code YWWZZZ

YY	WW	X	ZZ
year	working week assembly / packaging	plant identifier	free choice

Table 35. Start-up Revision Code

xx	Sequence
FF	engineering samples, no sequence programmed or sequence programmed on request
xx	customer specified sequence programmed during production test

Revision History

Revision	Date	Owner	Description
1.0	March, 2011	pkm	first official release

Note: Typos may not be explicitly mentioned under revision history.

12 Ordering Information

The devices are available as the standard products shown in Table 36.

Table 36. Ordering Information

Ordering Code	Marking	Description	Delivery Form	Package
AS3605-BQFR-FF	T1V2-FF	Multi Standard PMU - Engineering Samples	Tray	QFN40 5x5mm
AS3605-BQFP-xx	T1V2-xx	Multi Standard PMU - Production Parts Programmed	Tape and Reel (in dry pack)	QFN40 5x5mm

Note: All products are RoHS compliant and austriamicrosystems green.
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