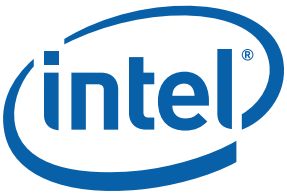

Intel® TXN31115D2 Quad-Rate 850 nm Optical Transceiver - SFP MSA Compatible

Datasheet

The Intel® LC Small Form Factor Pluggable (SFP) optical transceivers are high-performance integrated modules for bi-directional communication over Multimode optical fiber.

The Intel® TXN31115D2 Quad-Rate 850 nm Optical Transceiver (called hereafter the TXN31115D2 Optical Transceiver) is specifically designed for high-speed Fibre Channel data links at 4.25 Gbps (4x Fibre Channel rate). The TXN31115D2 Optical Transceiver is also backwards compatible with 2x and 1x Fibre Channel and Gigabit Ethernet rates.

The TXN31115D2 Optical Transceiver has an LC receptacle compatible with the industry-standard LC connector. The TXN31115D2 Optical Transceiver is Class 1 laser safety compliant with FDA Radiation Performance Standards, 21 CFR 1040.10, and international standards IEC 60825-1 and IEC 60825-2.

Product Features

- Compliant with the Fibre Channel FC-PI Standard
- 4.25/2.125/1.0625 Gbps Fibre Channel and 1.25 Gbps Ethernet Compatible
- Compatible with the SFP Multisource Agreement (MSA) Specification
- Hot pluggable
- 850 nm VCSEL emitter
- TTL Loss of Signal (LOS) Output
- Transmitter Disable Input
- AC-coupled CML Level Input/Output
- Single +3.3 V Power Supply
- Class 1 Laser Safety Product
- IEC/UL 60950-1 Safety Certified
- Designed and verified as RoHS compliant
- China RoHS compliant with 30-year EFUP
- Digital Diagnostics Support

Applications

- Fibre Channel Switch
- Fibre Channel Host Bus Adapter

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26-Sep-2007

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Revision History

Date	Revision	Description
26-Sep-2007	006	Updated parameters in Table 8, “Optical Specifications – Transmitter” on page 11. Change bars indicate areas of change.
09-Mar-2007	005	Modified “Electrical Characteristics – Receiver” - Text changed in rows for LOS output - Low and LOS output - High Modified “Optical Specifications – Transmitter” - Removed extinction ratio parameter Modified “Timing Parameters for SFP Management” - Removed Rate Select parameter Added “Electrical Characteristics – 2-Wire Interface” Added “Management Methods on Control of Pollution from Electronic Information Products (a.k.a. China RoHS)” Added “Hazardous Substances Table”
13-July-2006	004	“Electrical Characteristics – Power and Current” - Text changed “Optical Specifications – Receiver” - Text changed in rows for LOS - Asserted and LOS - De-asserted “Electromagnetic Compatibility Compliance” - Text changed
14-June-2006	003	“Absolute Maximum Ratings” - Text changed “Fiber Length Specifications” - Notes changed “Optical Specifications – Transmitter” - Text changed “A/D Fields – 2-Wire Address A2h, Addresses 96-109” - Text changed “Electromagnetic Compatibility Compliance” - Text changed
3-May-2006	002	“Electrical Characteristics – Transmitter” - Text changed “Optical Specifications – Receiver” - Text changed “Plug Sequence: Pin Engagement Sequence during Hot Plugging” - Notes changed “A/D Fields – 2-Wire Address A2h, Addresses 96-109” - Text changed “Electromagnetic Compatibility Compliance” - Text changed “Ordering Information” - Text and tables changed
17-Feb-2006	001	Initial release of document

1.0 Introduction

The Intel® TXN31115D2 Quad-Rate 850 nm Optical Transceiver - SFP MSA Compatible (called hereafter the TXN31115D2 Optical Transceiver) is specifically designed for high-speed Fibre Channel data links at 4.25 Gbps (4x Fibre Channel rate).

This document discusses the following TXN31115D2 Optical Transceiver topics:

For information on standards that apply to the TXN31115D2 Optical Transceiver, see the following references:

- “Diagnostic Monitoring Interface for Optical Xcvrs”. SFF Document Number SFF-8472, Revision 9.3.
- IEEE Std 802.3, 2002 Edition, Clause 38, PMD Type 1000BASE-SX. IEEE Standards Department, 2002
- IEEE Std 802.3z, 1998 Edition. Gigabit Interface Converter (GBIC) Ethernet Standard.
- Small Form-Factor Pluggable (SFP) Transceiver Multisource Agreement (MSA)
- Telcordia Technologies GR-63 Section 4.2

2.0 Specifications

Specifications include the following:

- Section 2.1, “Maximum Ratings and Recommended Operating Conditions” on page 8
- Section 2.2, “Electrical Characteristics” on page 9
- Section , “Table 5 lists the TXN31115D2 Optical Transceiver receiver electrical characteristics. Table 6 lists the TXN31115D2 Optical Transceiver 2-Wire Interface electrical characteristics. Optical Specifications” on page 10

2.1 Maximum Ratings and Recommended Operating Conditions

Table 1 lists the absolute maximum ratings for the TXN31115D2 Optical Transceiver.

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units	Notes
Storage Temperature	T_S	-40	–	85	°C	–
Relative Humidity	RH	5	–	95	%	–
Supply Voltage	$V_{cc}T$, R	-0.5	–	4	V	–
Data AC Voltage	TD+ and TD-	–	–	2.2	Vpp	Differential
Control Input Voltage	Vi	-0.5	–	Vcc + 0.3	V	–
Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.						

Table 2 lists the recommended operating conditions. (Minimum and maximum values listed in Table 3 through Table 9 apply over the recommended operating conditions specified in Table 2.)

Table 2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Case Temperature	T_c	-20	–	85	°C
Supply Voltage	$V_{cc}T$, R	2.97	3.3	3.63	VDC
Data Rate	–	1.0625	–	4.25	Gbps

2.2 Electrical Characteristics

The minimum and maximum values in this section apply over the following recommended temperature and voltage range (from Table 2, “Recommended Operating Conditions” on page 8).

-20 °C < Tc < 85 °C, 3.0 V < Vcc < 3.6 V

Table 3 lists the TXN31115D2 Optical Transceiver electrical characteristics for power and current.

Table 3. Electrical Characteristics – Power and Current

Parameter	Symbol	Min	Typ	Max	Units	Notes
Supply Current	I_{cc}	–	170		mA	T_c = 20°C, V_{cc} = 3.3 V
			–	220	mA	–
Power Dissipation	Pdiss	–	565	800	mW	–
Supply Noise Rejection	–	100	–	–	mV	10 kHz to 4 MHz with supply filter
Inrush Current	–	–	–	30	mA	Hot plugging of the TXN31115D2 Optical Transceiver results in the inrush current of no more than 30 mA greater than the steady state value.

Table 4 lists the TXN31115D2 Optical Transceiver transmitter electrical characteristics.

Table 4. Electrical Characteristics – Transmitter

Parameter	Symbol	Min	Typ	Max	Units	Notes
CML Input (Single Ended)	–	250	–	1100	mVpp	AC coupled inputs
CML Input (Differential)	–	500	–	2200	mVpp	Peak-to-peak voltage
Input Impedance (differential)	Z_{IN}	85	100	115	Ω	–
TX_DISABLE input voltage - High	V_{IH}	2	–	V_{cc} + 0.3	V	–
TX_DISABLE input voltage - Low	V_{IL}	0	–	0.6	V	–
TX_Fault Output Voltage - High	V_{OH}	2.0	–	Vcc + 0.3	V	IOH = 40 µA, 1 TTL Unit Load
TX_Fault Output Voltage - Low	V_{OL}	0	–	0.8	V	IOL = -1.6 mA, 1 TTL Unit Load

Table 5 lists the TXN31115D2 Optical Transceiver receiver electrical characteristics.

Table 5. Electrical Characteristics – Receiver

Parameter	Symbol	Min	Typ	Max	Units	Notes
CML Output (Single Ended)	–	250	300	500	mVpp	AC-coupled outputs
CML Output (Differential)	–	500	600	1000	mVpp	Peak-to-peak voltage
CML Output rise/fall time	–	–	–	115	ps	20% - 80%
Output Impedance (differential)	Zout	85	100	115	Ω	–
TTL LOS Output - Low	–	0	–	0.8	V	I_{OL} = -1.6 mA, 1 TTL Unit Load
TTL LOS Output - High	V_{OH}	2.0	–	V_{CC} + 0.3	V	I_{OL} = 40 µA, 1 TTL Unit Load
Deterministic Jitter	DJ			28.2	ps	–
Total Jitter	TJ	–	–	61.7	ps	–

Table 6 lists the TXN31115D2 Optical Transceiver 2-Wire Interface electrical characteristics. Optical Specifications

Table 6. Electrical Characteristics – 2-Wire Interface

Parameter	Symbol	Min	Typ	Max	Units	Notes
MOD_DEF (0:2)	V_{OH}	2.5	–	V_{CC} + 0.3	V	With Serial ID
	V_{OL}	0	–	0.5	V	–
	NC	100 K	–	–	Ω	Measured to RGND/ TGND

Table 7 lists the TXN31115D2 Optical Transceiver fiber length specifications.

Table 7. Fiber Length Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Data rate	BR		1.0625, 1.25, 2.125, 4.25		Gbps	1
Bit Error Rate	BER			10^{-12}		5
50 µm/125 µm MMF	L	2	–	500 300 150	m	2 3 4
62.5 µm/125 µm MMF	L	2	–	300 150 70	m	2 3 4

NOTES:
1. 1000BASE-SX compatible per IEEE802.3 and 1x, 2x, and 4x Fibre Channel compatible per FC-PI-2
2. Data rates at 1000BASE-SX Gigabit Ethernet and 1.0625 Gbps
3. Data rates at 2.125 Gbps Fibre Channel.
4. Data rate at 4.25 Gbps Fibre Channel.
5. Data rate at 4.25 Gbps with 2^7 - 1 PRBS pattern.

Table 8 lists the TXN31115D2 Optical Transceiver transmitter optical specifications.

Table 8. Optical Specifications – Transmitter

Parameter	Symbol	Min	Typ	Max	Units	Notes
Optical Transmit Power (50 or 62.5 µm MMF)	Popt	-8	-5	-2.5	dBm	Average launch power
Optical Center Wavelength		830	850	860	nm	–
Spectral Width	–	–	–	0.85	nm	RMS
Optical Modulation Amplitude	OMA	247	–	631	µW	pk-pk
Relative Intensity Noise	RIN	–	–	-118	dB/Hz	–
Deterministic Jitter	DJ			28.2	ps	–
Total Jitter	TJ	–	–	59.8	ps	–
Output Rise/Fall Time	tR, tF	–	–	90	ps	20 - 80% values, measured unfiltered
Eye Mask: Compliant with eye mask requirements of Fibre Channel – Physical Interfaces (FC-PI-2) specifications, IEEE 802.3z* Gigabit Ethernet 1000 BASE-SX standard						

Table 9 lists the TXN31115D2 Optical Transceiver receiver optical specifications.

Table 9. Optical Specifications – Receiver

Parameter	Symbol	Min	Typ	Max	Units	Notes
Optical Input Wavelength	–	770	–	860	nm	–
Receiver Sensitivity	Pr	-18	-20	–	dBm	1.0625 and 2.125 Gbps Test conditions: • 10^{-12} BER • 9 dB ER input • 2^7 - 1 PRBS
		-16	-18	–	dBm	4.25 Gbps Test conditions: • 10^{-12} BER • 9 dB ER input • 2^7 - 1 PRBS
Stressed Sensitivity	Compliant with Fibre Channel – Physical Interfaces (FC-PI-2) specifications, IEEE 802.3z Gigabit Ethernet 1000 BASE-SX standard					
Receiver Overload	–	–	–	0	dBm	–
Optical Return Loss	ORL	12	30	–	dB	–
LOS - Asserted	Pa	-29	–	–	dB	Measured on transition - low to high
LOS - De-asserted	Pd	–	–	-17	dBm	Measured on transition - high to low
LOS - Hysteresis	Pa - Pd	1	–	5	dB	–

3.0 Electrical Interface

Figure 1 shows the TXN31115D2 Optical Transceiver electrical interface pin numbers and names.

Figure 1. Electrical Interface Pin Numbers and Names

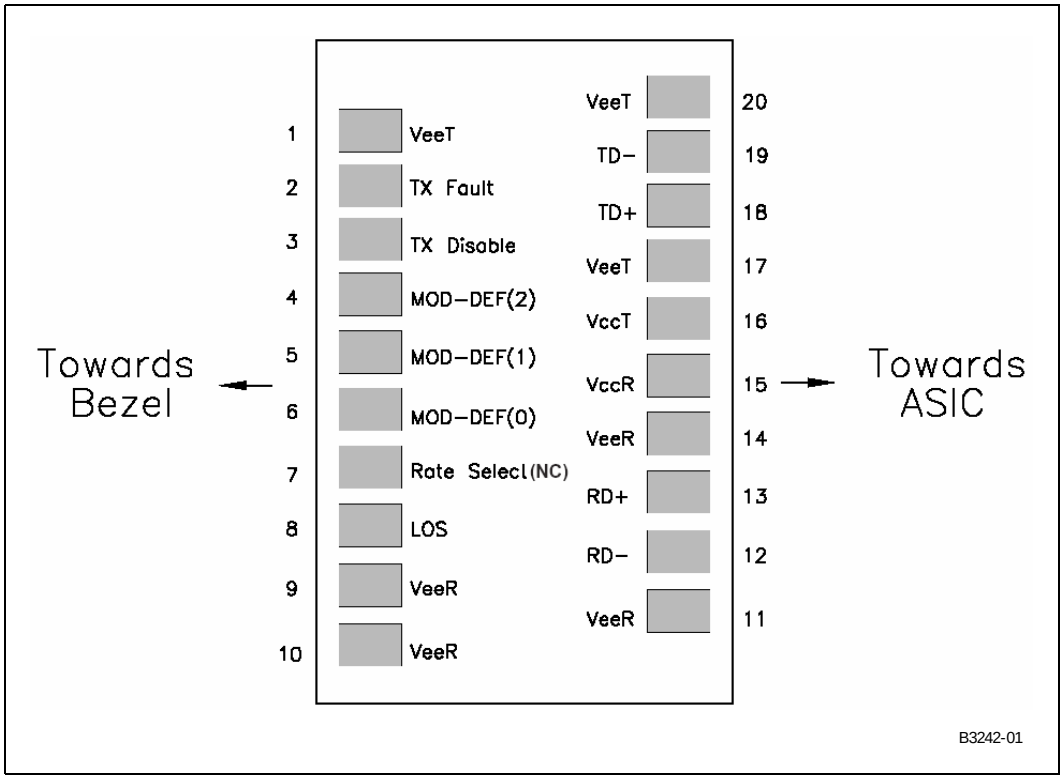


Table 10 lists the plug sequence to follow during hot plugging, as well as pin functions.

Table 10. Plug Sequence: Pin Engagement Sequence during Hot Plugging (Sheet 1 of 2)

Pin Number	Pin Name	Pin Function	Plug Sequence	Notes
1	$V_{ee}T$	Transmitter Ground	1	–
2	TX_FAULT	Transmitter Fault Indication	3	Note 1
3	TX_DISABLE	Transmitter Disable	3	Note 2: Transmitter disables on high or open
4	MOD_DEF (2)	Module Definition 2	3	Note 3: Wire Serial ID interface
5	MOD_DEF (1)	Module Definition 1	3	Note 3: Wire Serial ID interface
6	MOD_DEF (0)	Module Definition 0	3	Note 3: Ground
7	RATE SELECT	–	3	Note 4
8	LOS	Loss of Signal	3	Note 5
9	$V_{ee}R$	Receiver Ground	1	–
10	$V_{ee}R$	Receiver Ground	1	–
11	$V_{ee}R$	Receiver Ground	1	–

Table 10. Plug Sequence: Pin Engagement Sequence during Hot Plugging (Sheet 2 of 2)

Pin Number	Pin Name	Pin Function	Plug Sequence	Notes
12	RD-	Inverted Received Data out	3	Note 6
13	RD+	Non-Inverted Received Data out	3	Note 6
14	$V_{ee}R$	Receiver Ground	1	–
15	$V_{cc}R$	Receiver Power	2	Note 7
16	$V_{cc}T$	Transmitter Power	2	Note 7
17	$V_{ee}T$	Transmitter Ground	1	–
18	TD+	Non-inverted Data In	3	Note 8
19	TD-	Inverted Data In	3	Note 8
20	$V_{ee}T$	Transmitter Ground	1	–

NOTES:

1. TX FAULT is an open collector output that is pulled up with a 4.7 K - 10 K W resistor on the host board. Use a pull-up voltage between 2.0 V and $V_{cc}T$, R+0.3 V.
   - Low: Indicates normal operation. In the low state, the output is pulled to < 0.8 V.
   - High: Indicates a laser fault.
2. TX DISABLE is an input used to shut down the transmitter optical output. It is pulled up within the TXN31115D2 Optical Transceiver with a 4.7 K - 10 K W resistor. The states are as follows:
   - Low (0 - 0.6 V): Transmitter Enabled
   - (>0.8, <2.0 V): Undefined
   - High (2.0 - 3.465 V): Transmitter Disabled
3. MOD-DEF 0, 1, 2: These pins are definition pins for the TXN31115D2 Optical Transceiver. They are pulled up with a 4.7 K - 10 K W resistor on the host board. Use a pull-up voltage between 2.0 V and $V_{cc}T$, R+0.3 V.
   - MOD-DEF 0 is grounded by the TXN31115D2 Optical Transceiver to indicate the TXN31115D2 Optical Transceiver is present.
   - MOD-DEF 1 is the clock line of a two-wire serial interface for serial ID.
   - MOD-DEF 2 is the data line of a two-wire serial interface for serial ID.
4. RATE SELECT: This signal function is not implemented in the TXN31115D2 Optical Transceiver. The TXN31115D2 Optical Transceiver is rate agile – that is, it meets the specifications for 1.0625 Gbps to 4 Gbps data rates without the use of a rate-select pin.
5. LOS (Loss of Signal) is an open collector output that is pulled up with a 4.7K – 10KW resistor on the host board.
   - When low, this output indicates normal operation. In the low state, the output is pulled to < 0.8V.
   - When high, this output indicates the received optical power is below the worst-case receiver sensitivity (as defined by the standard in use).
6. RD-/+ are the differential receiver outputs. They are AC-coupled 100 W differential lines that are terminated with 100 W (differential) at the user SerDes. The AC coupling is performed inside the TXN31115D2 Optical Transceiver and is therefore not required on the host board.
7. $V_{cc}R$ and $V_{cc}T$ are the receiver and transmitter power supplies. Their values, which are listed in Table 2, "Recommended Operating Conditions" on page 8, are defined at the SFP connector pin. Maximum supply current is listed in Table 3, "Electrical Characteristics – Power and Current" on page 9. Hot plugging of the TXN31115D2 Optical Transceiver results in the inrush current listed in Table 3, "Electrical Characteristics – Power and Current" on page 9.
8. TD-/+ are the differential transmitter inputs. They are AC-coupled differential lines with 100 W differential termination inside TXN31115D2 Optical Transceiver. The AC coupling is performed inside the TXN31115D2 Optical Transceiver and is therefore not required on the host board.

4.0 Termination

4.1 Types of I/O Interfaces

The TXN31115D2 Optical Transceiver has the following types of I/O interfaces.

- CML interface
- TTL interface

High-speed I/Os use the CML interface, while control signals use the TTL interface. Proper termination of I/Os is required for good signal integrity. If I/Os (particularly the CML I/Os) are not terminated properly, then jitter increases significantly due to reflection from impedance mismatches.

4.2 CML Termination

Figure 2 shows a circuit diagram for the CML termination for the TXN31115D2 Optical Transceiver receiver output. The TXN31115D2 Optical Transceiver has built in AC-coupling capacitors, which help prevent a direct current path from the TXN31115D2 Optical Transceiver power supply to the SerDes input. (A direct current path could damage the ESD diodes on the SerDes.)

- **Internal termination.** For the TXN31115D2 Optical Transceiver receiver output, the SerDes interface provides an internal termination resistor.
- **External termination.** For the proper external termination of the SerDes interface, refer to the SerDes specification.

Figure 2. Circuit Diagram for CML Termination on Receiver Output

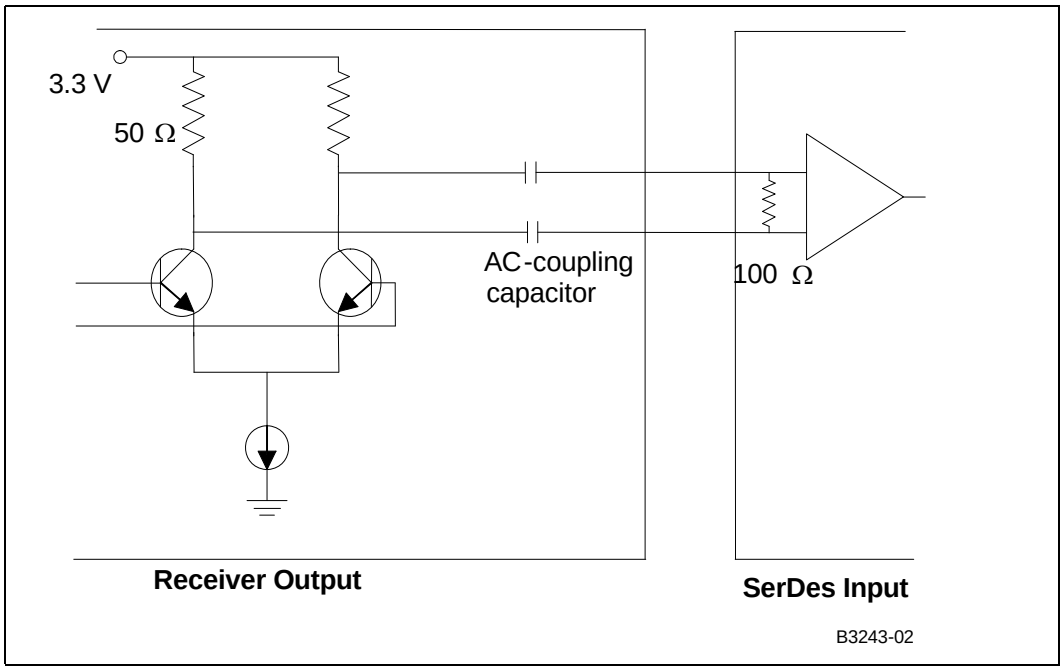
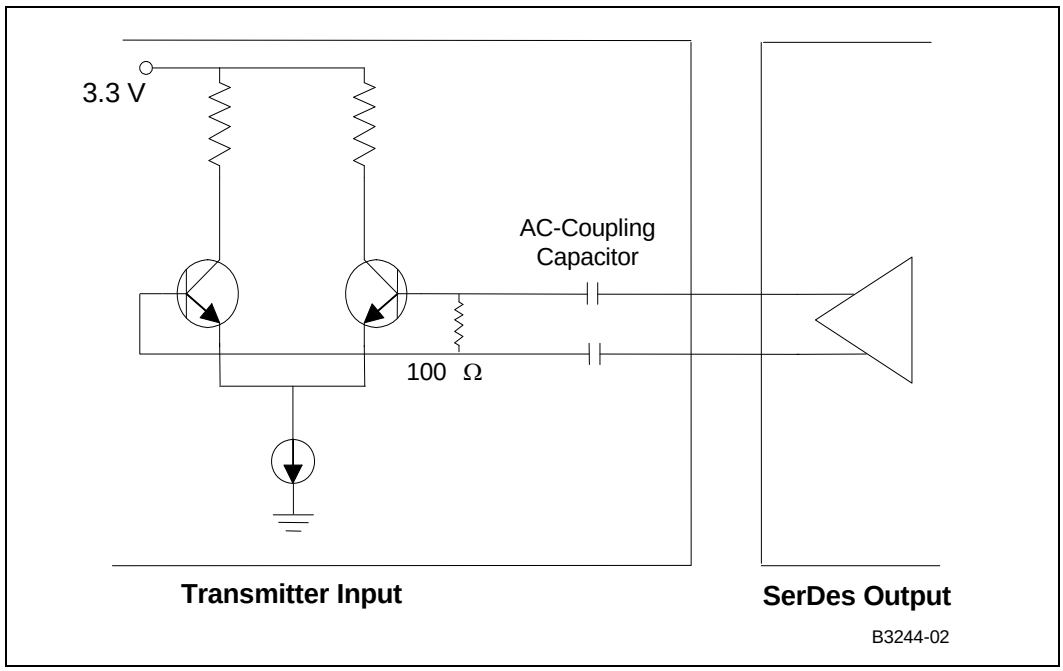


Figure 3 shows a circuit diagram for the CML termination for the TXN31115D2 Optical Transceiver transmitter input.

Internal termination. The TXN31115D2 Optical Transceiver transmitter input has an internal 100 Ω termination between two inputs. AC-coupling capacitors are also built into the TXN31115D2 Optical Transceiver.

Figure 3. Circuit Diagram for CML Termination on Transmitter Input



5.0 SFP Timing Parameters

Table 11 lists the timing parameters for SFP management.

Table 11. Timing Parameters for SFP Management

Parameter	Symbol	Min	Max	Unit	Conditions
TX_DISABLE assert time	t_off	–	10	µs	Time from rising edge of TX_DISABLE to when the optical output falls below 10% of nominal
TX_DISABLE negate time	t_on	–	1	ms	Time from falling edge of TX_DISABLE to when the modulated optical output rises above 90% of nominal
Time to initialize includes reset of TX_FAULT	t_init	–	300	ms	Time from power on or negation of TX_FAULT using TX_DISABLE
TX_FAULT Assert Time	t_fault	–	100	µs	Time from fault to TX_FAULT ON
TX Disable to reset	t_reset	10		µs	Time TX Disable must be held high to reset TX_FAULT
RX_LOS Assert time	t_loss_on	–	100	µs	Time from LOS state to RX_LOS assert
RX_LOS De-assert time	t_loss_off	–	100	µs	Time from non-LOS state to RX_LOS de-assert
Serial ID Clock Rate	f_serial_clock	–	100	kHz	–

6.0 Digital Diagnostic Monitoring Interface

This section includes the following topics:

6.1 Overview of Digital Diagnostic Monitoring Interface

The TXN31115D2 Optical Transceiver supports the 2-wire serial communication protocol. The TXN31115D2 Optical Transceiver has a digital diagnostic monitoring interface that is an extension of the serial ID interface defined in the Gigabit Interface Converter (GBIC) specification and the SFP Transceiver MultiSource Agreement (MSA) referenced in Section 1.0, “Introduction” on page 7.

- **Standard SFP serial ID interface.** The standard SFP serial ID interface (the memory map for which is in Table 12, “Memory Map – 2-Wire Address Range Descriptions” on page 18) provides access to identification information using the 8-bit address 1010000X (A0h). The serial identification information describes information such as the following for the TXN31115D2 Optical Transceiver: capabilities, standard interfaces, and manufacturer information.
- **Digital diagnostic monitoring interface.** The digital diagnostic monitor interface (the memory map for which is in Table 12, “Memory Map – 2-Wire Address Range Descriptions” on page 18) is an extension of the standard serial ID interface. This interface, which uses the 8-bit address 1010001X (A2h) reserved for optical transceivers, allows real-time access to device-operating parameters while leaving unchanged the original serial ID memory map A0h. The digital diagnostic monitoring interface is backward compatible with both the GBIC specification and the SFP MSA.

Note: For details on the 2-wire addresses A0h and A2h, refer to the SFF-8472 document referenced in Section 1.0, “Introduction” on page 7.

6.2 General Memory Map Descriptions

Table 12 lists descriptions of address ranges for the serial ID memory map.

- The 2-wire address A0h contains serial ID information defined by the SFP MSA.
- The 2-wire address A2h contains data related to the digital diagnostics, defined by the SFF-8472 document referenced in Section 1.0, "Introduction" on page 7.

Table 12. Memory Map – 2-Wire Address Range Descriptions

2-Wire Address 1010000X (A0h)		2-Wire Address 1010001X (A2h)	
Address Range	**Address Range Description (Standard Serial ID Information)**	**Address Range**	**Address Range Description (Digital Diagnostics Information)**
0-95	Serial ID Defined SFP MSA (96 bytes)	0-39	Alarm and Warning (40 bytes) For details, see Table 13, "Alarm and Warning Fields – 2-Wire Address A2h, Address 0-95".
		40-95	Vendor Specific / Calibration Constants (56 bytes) For details, see Table 13, "Alarm and Warning Fields – 2-Wire Address A2h, Address 0-95".
96-127	Vendor Specific (32 bytes)	96-119	Real Time Digital Diagnostics Interface (24 bytes) For details, see the following: • Table 14, "A/D Fields – 2-Wire Address A2h, Addresses 96-109" on page 21 • Table 15, "A/D Status/Control Bits – 2-Wire Address A2h, Address 110" on page 21
		120-127	Vendor Specific (8 bytes)
128-255	Reserved in SFP MSA (128 bytes)	128-247	User Writable EEPROM (120 bytes)
		248-255	Vendor Specific (8 bytes)

6.3 Alarm and Warning Fields for 2-Wire Interface Address A2h

Table 13 is a more detailed memory map of the 2-wire interface address A2h for the Alarm and Warning fields, address range 0 to 95.

Table 13. Alarm and Warning Fields – 2-Wire Address A2h, Address 0-95 (Sheet 1 of 2)

Data Address	Field Size (Bytes)	Field Name	Field Description
Base ID Fields			
0	1	Temperature High alarm	MSB at low address
1	1	LSB	MSB at low address
2	1	Temperature Low alarm	MSB at low address
3	1	LSB	MSB at low address
4	1	Temperature High Warning	MSB at low address
5	1	LSB	MSB at low address
6	1	Temperature Low Warning	MSB at low address
7	1	LSB	MSB at low address
8	1	Vcc High Alarm	MSB at low address
9	1	LSB	MSB at low address
10	1	Vcc Low Alarm	MSB at low address
11	1	LSB	MSB at low address
12	1	Vcc High Warning	MSB at low address
13	1	LSB	MSB at low address
14	1	Vcc Low Warning	MSB at low address
15	1	LSB	MSB at low address
16	1	Bias High Alarm	MSB at low address
17	1	LSB	MSB at low address
18	1	Bias Low Alarm	MSB at low address
19	1	LSB	MSB at low address
20	1	Tx Bias High Warning	MSB at low address
21	1	LSB	MSB at low address
22	1	Tx Bias Low Warning	MSB at low address
23	1	LSB	MSB at low address
24	1	Tx Power High Alarm	MSB at low address
25	1	LSB	MSB at low address
26	1	Tx Power Low Alarm	MSB at low address
27	1	LSB	MSB at low address
28	1	Tx Power High Warning	MSB at low address
29	1	LSB	MSB at low address
30	1	Tx Power Low Warning	MSB at low address
31	1	LSB	MSB at low address
32	1	Rx Power High Alarm	MSB at low address
33	1	LSB	MSB at low address

Table 13. Alarm and Warning Fields – 2-Wire Address A2h, Address 0-95 (Sheet 2 of 2)

Data Address	Field Size (Bytes)	Field Name	Field Description
34	1	Rx Power Low Alarm	MSB at low address
35	1	LSB	MSB at low address
36	1	Rx Power High Warning	MSB at low address
37	1	LSB	MSB at low address
38	1	Rx Power Low Warning	MSB at low address
39	1	LSB	MSB at low address
40-55	16	Vendor-Specific	–
56-95	40	Calibration Constants	–

6.4 A/D Fields for 2-Wire Interface Address A2h

Table 14 lists descriptions of the analog-to-digital (A/D) fields for the 2-wire interface address A2h, data addresses 96 to 109.

Table 14. A/D Fields – 2-Wire Address A2h, Addresses 96-109

Data Address	Field Size (Bytes)	Field Name	Field Description
96	1	Temperature MSB	Signed 2's complement integer ºC (-40 to +125). Based on internal temperature measurement.
97	1	Temperature LSB	Fractional part of temperature (count/256)
98	1	Vcc MSB	Internally measured supply voltage in transceiver. Voltage reading is full 16-bit value × 100 µVolt. (Yields range of 0 to 6.55V)
99	1	Vcc LSB	
100	1	TX Bias MSB	Measured Laser Bias Current in mA. Bias current is full 16-bit value × 2 µA. (Full range of 0 to +131 mA)
101	1	TX Bias LSB	
102	1	TX power MSB	Measure TX output power in mW. TX power is full 16-bit value × 0.1 µW. (Full range of -40 to +8.2 dBm)
103	1	TX power LSB	
104	1	RX Power MSB	Measured RX input power in mW. RX power is full 16-bit value × 0.1 µW. (Full range of -40 to +8.2dBm)
105	1	RX Power LSB	
106-109	4	Reserved	–

Table 15 lists descriptions of the A/D status/control bits for the 2-wire interface address A2h, data address 110.

Table 15. A/D Status/Control Bits – 2-Wire Address A2h, Address 110

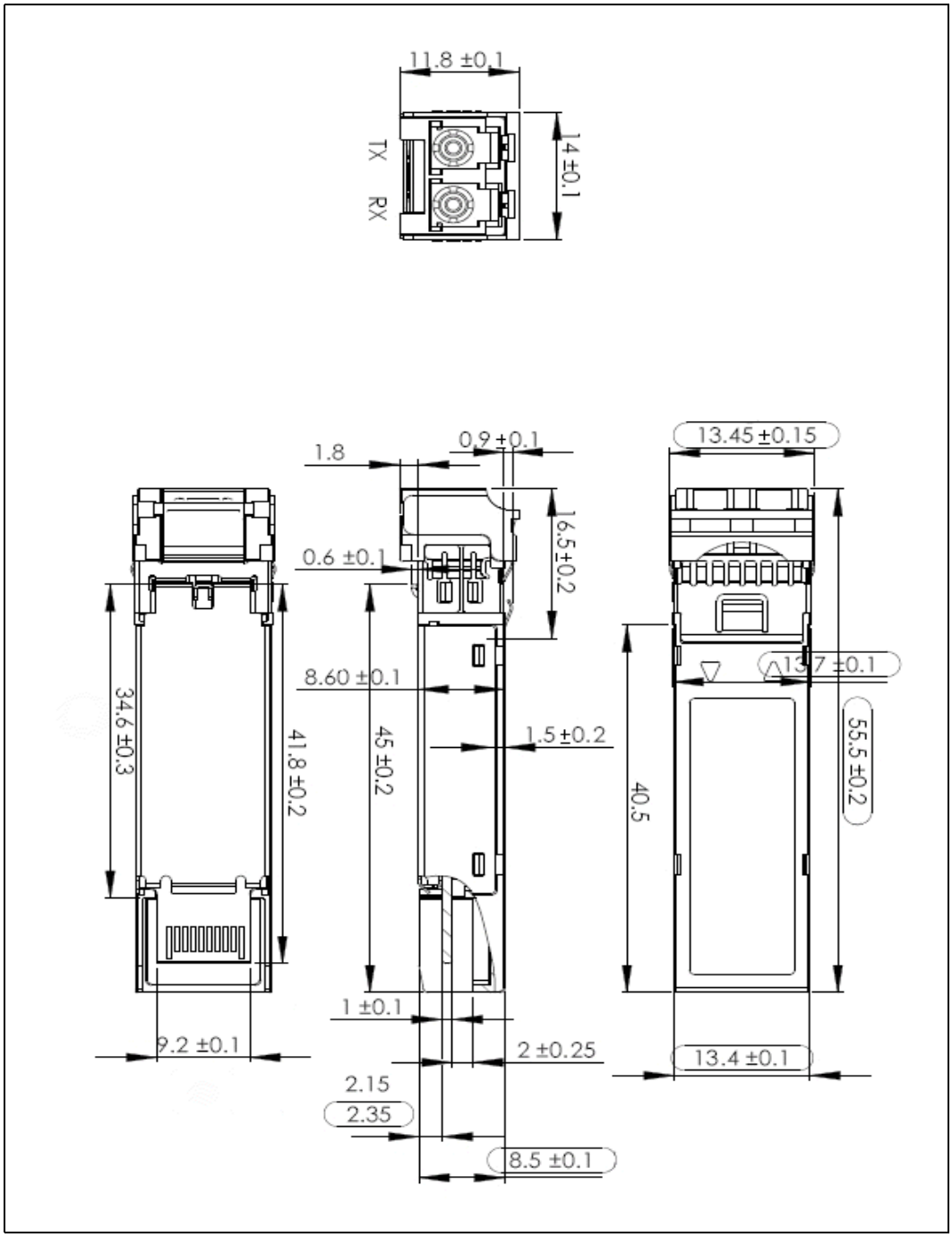
Data Address	Bit	Bit Name	Bit Description
110	2	Tx Fault	Digital State of Tx Fault Output
110	1	LOS	Digital State of LOS
110	0	Data Ready Bar	Indicates transceiver has achieved power up and is ready.

7.0 Mechanical Specification

Figure 4 shows the TXN31115D2 Optical Transceiver SFP mechanical specifications. The dimensions comply with the SFP Multisource Agreement (MSA).

Note: Aqueous wash is not applicable for this product.

Figure 4. SFP Mechanical Specifications



8.0 Regulatory Compliance

This section discusses the following topics:

8.1 Electromagnetic Compatibility Compliance

Table 16 lists emissions and immunity regulations with which the TXN31115D2 Optical Transceiver complies.

Table 16. Electromagnetic Compatibility Compliance

Requirement	Regulation	Performance Level
Electromagnetic interference (EMI)	• FCC rules, Part 15, subpart B • EN 55022	Meets Class B limits with a minimum 6 dB margin
Electrostatic discharge (ESD)	JEDEC JESD22-A114-B Human Body Model	± 2 kV contact discharge to connector electrical pins with no degradation in performance or loss of function
	EN 61000-4-2	• ± 15 kV air discharge • ± 8 kV contact discharge to face plate Meets Level B test criteria (that is, no degradation of performance or loss of function occurs). ***Note:*** Actual ESD may vary, depending on system configuration.
Radio frequency electromagnetic field (Radiated immunity)	EN 61000-4-3, Level A test criteria	10 V/m from 80 MHz to 1 GHz with no degradation of performance or loss of function

8.2 Safety Compliance

Table 17 lists and describes the relevant safety regulations with which the TXN31115D2 Optical Transceiver complies.

Table 17. Safety Compliance

Requirement	Regulation	Title
Product Safety	UL 60950-1 CSA C22.2 No. 60950-1	Information Technology Equipment – Safety - Part 1: General Requirements (USA and Canada)
	EN 60950-1+A11	Information Technology Equipment – Safety - Part 1: General Requirements (European Union)
	IEC 60950-1	Information Technology Equipment – Safety - Part 1: General Requirements (International)
	GR-63-CORE Section 4.2, Clause 4.2.3.1	Compliant with the fire resistance requirements of Telcordia Technologies Generic Requirements GR-63-CORE document for discrete electronic components.
Laser Safety	21CFR1040.10	Code of Federal Regulations Title 21 Chapter I Subchapter J – Radiological Health Part 1040: Performance Standards for Light-Emitting Products
	EN 60825-1+A1 +A2	Safety of Laser Products - Part 1: Equipment Classification, Requirements and User's Guide
	IEC 60825-1 +A1 +A2	Safety of Laser Products - Part 1: Equipment Classification, Requirements and User's Guide
	EN 60825-2	Safety of Laser Products - Part 2: Safety of Optical Fiber Communication Systems
	IEC 60825-2	Safety of Laser Products - Part 2: Safety of Optical Fiber Communication Systems

Caution: This device is a Class 1 laser product for use only under the recommended operating conditions and ratings specified in this document.

Use of controls or adjustments or performance of procedures other than these specified in this product datasheet may result in hazardous radiation exposure.

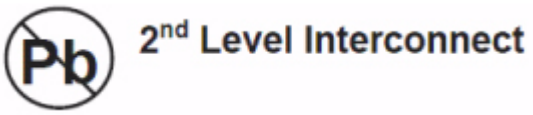
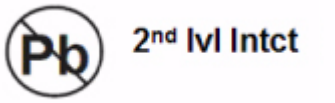
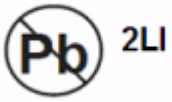
This device complies with 21 CFR 1040.10 except for deviations pursuant to Laser Notice No. 50 dated July 26, 2001.

8.3 Lead-Free Conformance

The TXN31115D2 Optical Transceiver uses a lead-free assembly, although certain discrete components within the assembly may contain lead, being necessary for either component performance or reliability. The TXN31115D2 Optical Transceiver is referred to as a "Lead-free 2nd Level Interconnect." The enclosure, circuit board substrate, and the solder connections from the circuit board to the components (second-level connections) are all lead-free.

Table 18 lists various forms of the "Lead-Free 2nd Level Interconnect" marking for the TXN31115D2 Optical Transceiver and accompanying collateral.

Table 18. Lead-Free 2nd-Level Interconnect Markings

Description	Marking
Lead-Free 2nd Level Interconnect: The Lead-Free 2nd Level Interconnect symbol is used to identify electrical and electronic assemblies and components in which the lead (Pb) concentration level in the circuit board substrate and the solder connections from the circuit board to the components (second-level interconnect) are not greater than 0.1% by weight (1000 ppm). ***Note:*** Any of the three symbols shown may be used, as space permits.	 or  or 

8.4 Compliance with Restriction of Hazardous Substances

This product complies with the European Union directive for Restriction of Hazardous Substances (RoHS) – *Restriction on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment*, Directive 2002/95/EC plus amendments.

However, certain discrete components do contain lead (a RoHS-restricted substance) in amounts that exceed threshold concentration levels. This product uses the following applicable RoHS technology exemptions:

- Lead in optical and filter glass
- Lead in glass of electronic components
- Lead in electronic ceramic parts

Note: RoHS implementation details are subject to change.

This product is RoHS 6 compliant, defined as complying with the restriction for all six listed substances by meeting strict threshold levels for those substances or through the use of the applicable exemptions listed above.

8.5 Management Methods on Control of Pollution from Electronic Information Products (a.k.a. China RoHS)

关于符合中国《电子信息产品污染控制管理办法》的声明

Table 19. Hazardous Substances Table

产品中有毒有害物质的名称及含量

部件名称 (Parts)	有毒有害物质或元素 (Hazardous Substance)					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
集成光电器件 Integrated optical circuit board assembly	×	○	○	○	○	○
金属盒件 Metal enclosure	○	○	○	○	○	○

○：表示该有毒有害物质在该部件所有均质材料中的含量均在SJ/T 11363-2006标准规定的限量要求以下。

○： Indicates that this hazardous substance contained in all homogeneous materials of this part is below the limit requirement in SJ/T 11363-2006.

×：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出SJ/T 11363-2006标准规定的限量要求。

×： Indicates that this hazardous substance contained in at least one of the homogeneous materials of this part is above the limit requirement in SJ/T 11363-2006.

对销售之日的所售产品，本表显示我公司供应链的电子信息产品可能包含这些物质。注意：在所售产品中可能会也可能不会含有所有所列的部件。

This table shows where these substances may be found in the supply chain of our electronic information products, as of the date of sale of the enclosed product. Note that some of the component types listed above may or may not be a part of the enclosed product.

除非另外特别的标注，此标志为针对所涉及产品的环保使用期限标志. 此环保使用期限只适用于产品在产品手册中所规定的条件下工作.

The Environment-Friendly Use Period (EFUP) for all enclosed products and their parts are per the symbol shown here, unless otherwise marked. The Environment-Friendly Use Period is valid only when the product is operated under the conditions defined in the product manual.

8.6 Product Certification Markings and Compliance Statements

Table 20 lists the TXN31115D2 Optical Transceiver product certification markings and compliance statements.

Table 20. Product Certification Markings and Compliance Statements

Origin and Description	Markings and Compliance Statements
Markings	
CE mark. The CE (Conformité Européene*) mark indicates compliance to the European Union Low Voltage directive (2006/95/EC, formerly 73/23/EEC).	
TÜV Rheinland type approval mark for components and subassemblies for the European Union. The Technischer Überwachungsverein* (TÜV – German for "Technical Inspection Association") Rheinland type approval mark is for components and subassemblies for the European Union. Where space does not permit, the smaller alternate TÜV mark (see the next row in this table) may be used.	
TÜV Rheinland type approval mark for components and subassemblies for the European Union – *Alternate*. This alternate mark may be used where space constraints exist that do not permit use of the TUV Rheinland mark in the previous row of this table.	Alternate TÜV mark: 
UL Recognized Component mark for the USA and Canada.	
China Environmental Friendly Use Period (EFUP) mark, where 30 in the marking denotes 30 years. The number provided as the EFUP is provided solely to comply with applicable laws of the People's Republic of China. It does not create any warranties or liabilities on behalf of Intel Corporation to customers.	
Compliance Statements	
USA Food and Drug Administration (FDA), Center for Devices and Radiological Health compliance statement.	Complies with 21CFR 1040.10 except for deviations pursuant to Laser Notice No. 50, dated July 26, 2001.
USA FDA, Center for Devices and Radiological Health compliance statement – *Alternate*. Use the alternate statement listed, as needed.	Alternate FDA compliance statement: Complies with FDA performance standards for laser products except for deviations pursuant to Laser Notice No. 50, dated July 26, 2001.

9.0 Ordering Information

Table 21 lists ordering information for the TXN31115D2 Optical Transceiver.

Table 21. Ordering Information

Product Number	MM Number	Description
TXN31115D200xxx[1]	874223	Quad-rate 4/2/1 Gbps Fibre Channel and Gigabit Ethernet SFP module with digital diagnostics feature compliant with RoHS 6

1. The last 3 characters of the part number ("xxx") are used to designate customer-specific customization. The Intel standard part has "000" as the last three characters.

10.0 Acronyms

Table 23. Acronyms

Acronym	Meaning
A/D	Analog-to-Digital
BER	Bit Error Rate
CFR	Code of Federal Relations
CML	Current Mode Logic
EMI	Electro-Magnetic Interference
ESD	Electro-Static Discharge
EU	European Union
FC-PI	Fibre Channel – Physical Interfaces
FCC	Federal Communications Commission
FDA	Food and Drug Administration
GBIC	GigaBit Interface Converter
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
LOS	Loss of Signal
MMF	Multimode Fiber
MSA	Multisource Agreement
NRZ	Non-Return to Zero
Pb	Lead
PCB	Printed Circuit Board
PRBS	Pseudo Random Bit Sequence
RFI	Radio Frequency Immunity
SFF	Small-Form Factor
SCSI	Small Computer System Interface
SONET	Synchronous Optical Network
TOSA	Transmitter Optical Sub-Assembly
TTL	Transistor-Transistor Logic
TUV	Technischer Überwachungsverein
UL	Underwriter Laboratories*
VCSEL	Vertical Cavity Surface Emitting Laser

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