Arria V GX FPGA Development Kit

from *Altera*

The Altera® Arria® V GX FPGA Development Kit provides a complete design environment that includes all the hardware and software that you need to develop full FPGA designs and test them within a system environment. The development kit is RoHS compliant. The development kit includes the following features:

- Two FPGAs for system level design
- Arria V GX—360KLE, F1517 package, 24X6G XCVRs, C6 speed grade
- Three I/O expansion slots—Two high-speed mezzanine cards (HSMCs) and one FMC
- 2 GB of SDRAM memory, 4.5 MB of QDR II memory, and 512 MB of flash memory
- Display port and SFP+ connections
- SMAs and the new Samtec Bullseye
- Amphenol® connectors for signal integrity (SI) and backplane measurements
- Ability to measure individual power rails on each chip

Ordering Information

Table 1. Altera's Arria V GX FPGA Development Kit Ordering Information (1)

Ordering Code	Price	Ordering Information
DK-DEV-5AGXB3N/ES		The **Arria V GX FPGA Development Kit** features a 5AGXB3 Engineering Sample (ES) device and a 1-year license for the Quartus® II design software. Contact your local Altera distributor to place your order.

Note:

1. You can purchase optional HSMC connector interface-compatible daughtercards, adapters, or cables to use with your development kit.

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Development Kit Contents

The Arria V GX FPGA Development Kit features the following:

- Arria V GX FPGA development board (see Figure 1)
- Unit 1: Arria V GX FPGA: 5AGXFB3H6F40C6NES
  - Memory
    - 1,152 MB x 72 DDR3 SDRAM
    - 4.5 MB (1Mb x 36) QDR II+ SRAM
    - 64 MB sync flash (x16)
  - Communication Ports
    - PCIe x8 edge connector
    - HSMC Port A (Four transceiver channels)
    - USB 2.0
    - Gigabit Ethernet
    - Chip-to-chip bridge with 30 LVDS inputs and 30 LVDS outputs, and x8 XCVRs
    - One SFP+ channel
    - Bullseye connector (x1 channel)
    - SMA connectors (x1 channel)
  - Configuration
    - JTAG

        - Fast passive parallel (FPP) parallel flash loader (PFL)
    - Buttons, Switches, LEDs, Displays
        - One reset config pushbutton
        - One CPU reset pushbutton
        - Three user pushbuttons
        - Two configuration pushbuttons
        - Eight dip switches
        - 16 user LEDs (eight bi-color diodes)
        - 16x2 character LCD
- Unit 2: Arria V GX FPGA: 5AGXFB3H6F40C6NES
    - Memory
        - x64 DDR3 SDRAM Soft Controller (x32 hard IP controller)
    - Communication Ports
        - HSMC Port B (Four transceiver channels)
        - FMC Port (Four transceiver channels)
        - Chip-to-chip bridge with 30 LVDS inputs and 30 LVDS outputs, and x8 XCVRs
        - One serial digital interface (SDI) channels
        - Backplane connector (Four transceiver channels)
        - Bullseye connector (One transceiver channel)
        - SMA connector (One transceiver channel)
    - Configuration
        - JTAG
        - Fast passive parallel PFL
    - Buttons, Switches, LEDs, Displays
        - One CPU reset pushbutton
        - Three user pushbuttons
        - Eight dip switches
        - 16 user LEDs (eight bi-color diodes)
- Misc
    - EPM2210F324 system controller
    - EPM570GM100 on-board USB-Blaster™ II
- Clocking
    - 50-MHz, 100-MHz, and 125-MHz programmable oscillators
    - SMA input (LVPECL)
- Power
    - Laptop DC Input
    - PCI Express® (PCIe®) edge connector
- System Monitoring
    - Power (voltage, current, wattage)—Per unit per rail
    - Temperature (per FPGA die, local board)
- Loopback and debug HSMC cards
- Power adapter and cables
- Arria V GX FPGA Development Kit software content
    - Complete documentation
        - User guide
        - Reference manual
        - Board schematics and layout design files
    - GUI-based Board Test System
        - Includes complete Quartus II projects with open source register transfer level (RTL)
    - Board Update Portal
        - Includes complete Quartus II projects with open source RTL
    - Quartus II design software, Development Kit Edition (DKE)
        - License to use full version of Quartus II software for one year
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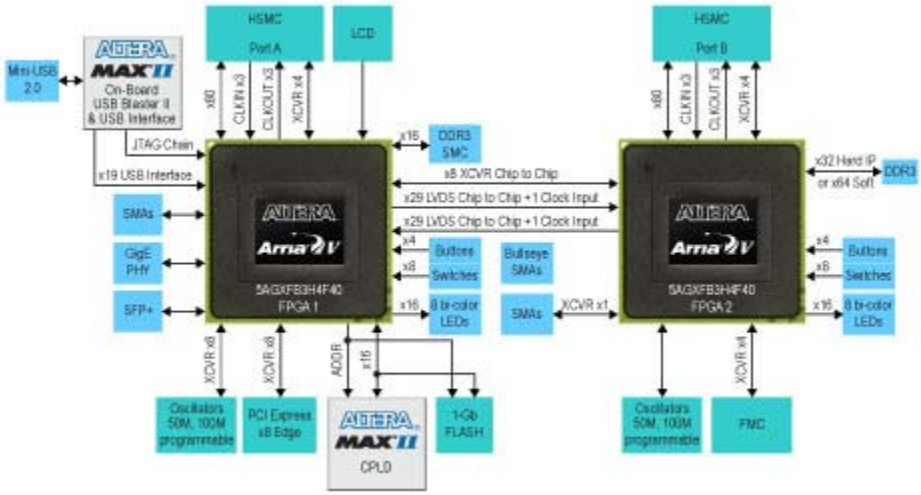
Figure 1. Arria V GX FPGA Development Board with an 5AGXB3ES FPGA Device

Figure 2. Arria V GX FPGA Development Board Block Diagram



Related Links

- Arria V FPGA documentation page
- *Errata Sheet and Guidelines for Arria V ES Devices* (PDF)
- Altera and partner daughter cards
- Other Arria V FPGA-based development kits
- Jungo PCI Express WinDriver (30-day evaluation)